PM920030181 US1
1/50
BENDER ET AL

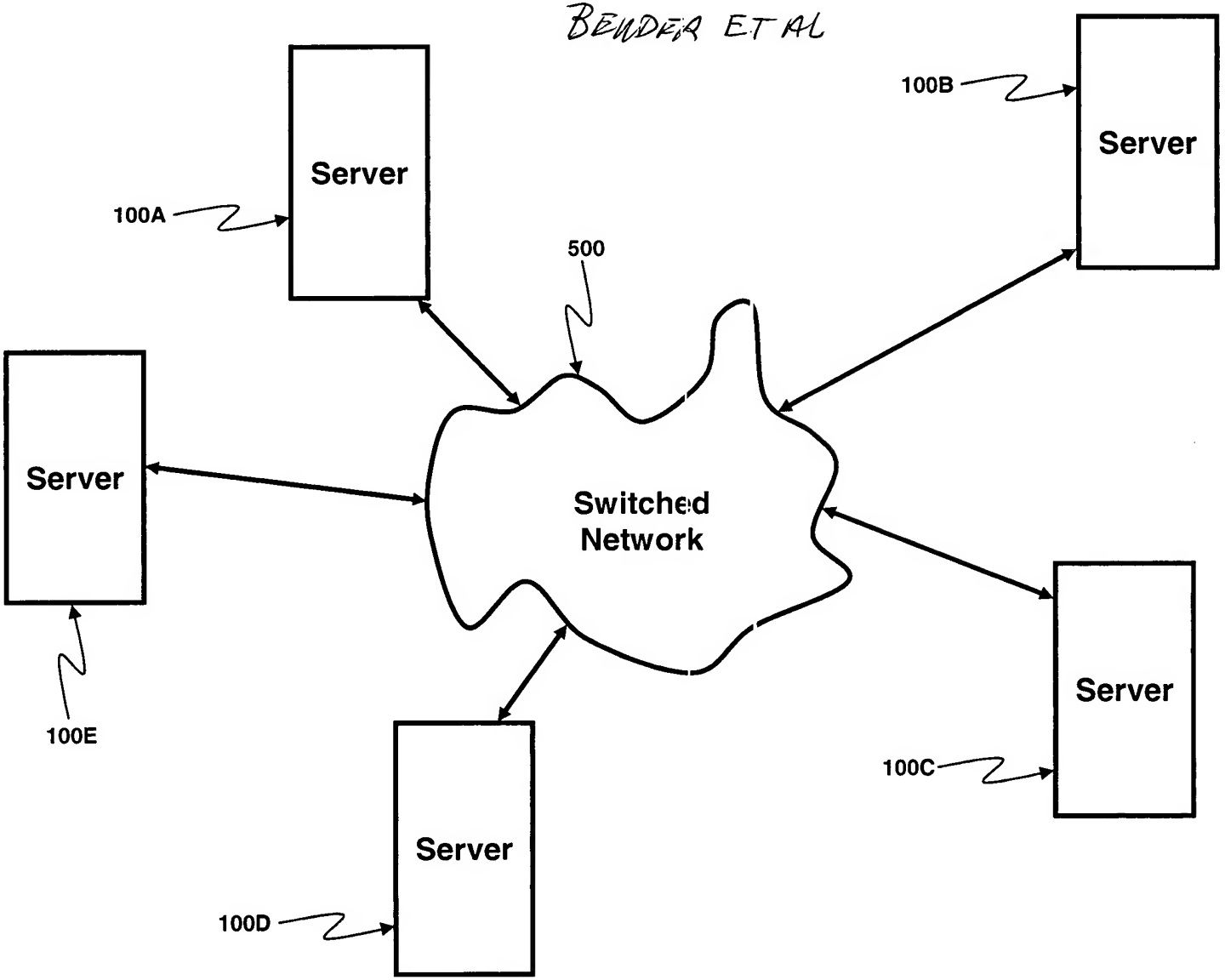


Figure 1

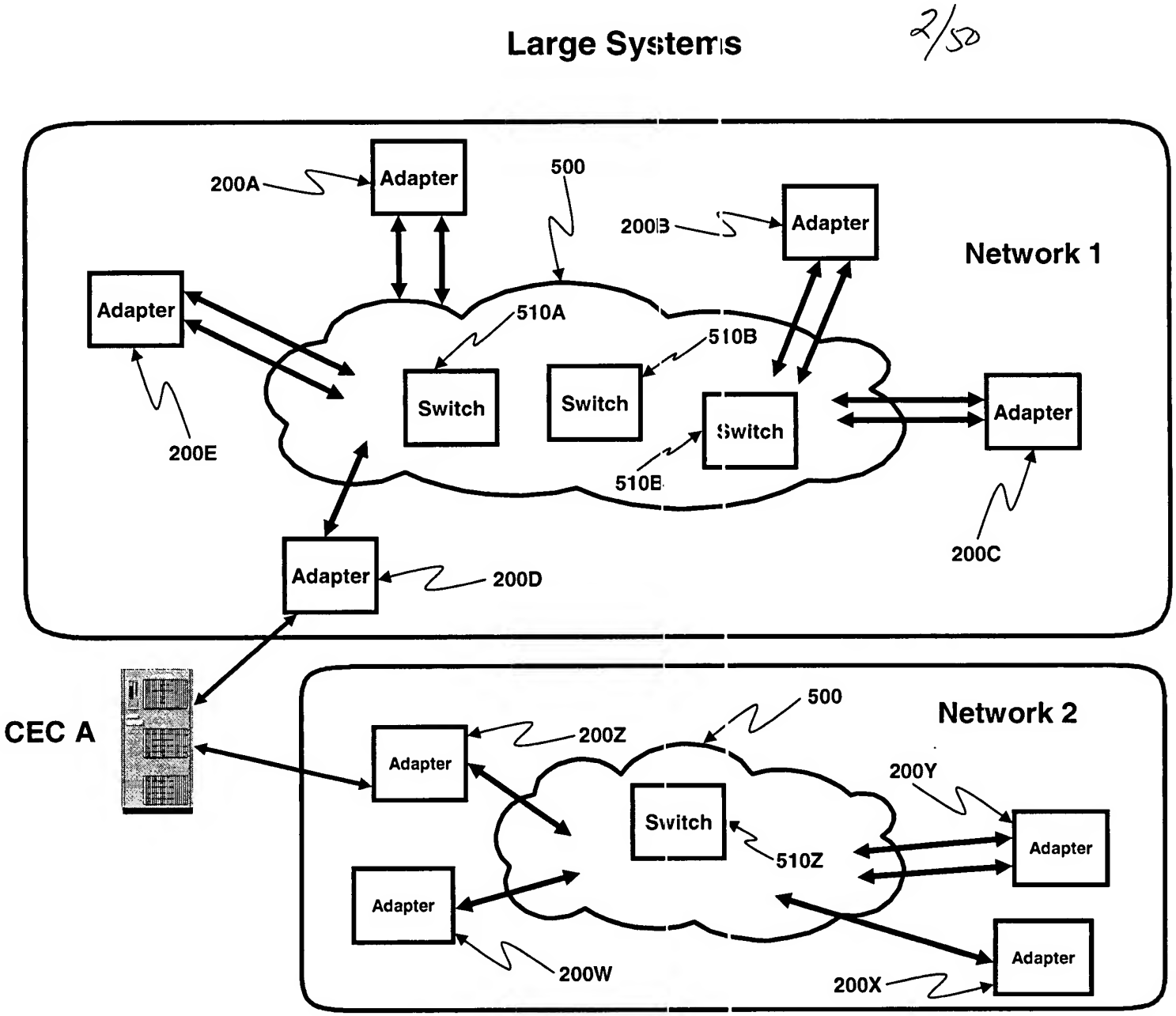

Large Systems
200A
Adapter
500
200B
Adapter
Network 1
Adapter
510A
510B
Switch
Switch
Switch
Adapter
200E
510B
200C
Adapter
200D
CEC A
500
Network 2
200Z
Adapter
200Y
Switch
510Z
Adapter
Adapter
Adapter
200W
200X

Figure 2

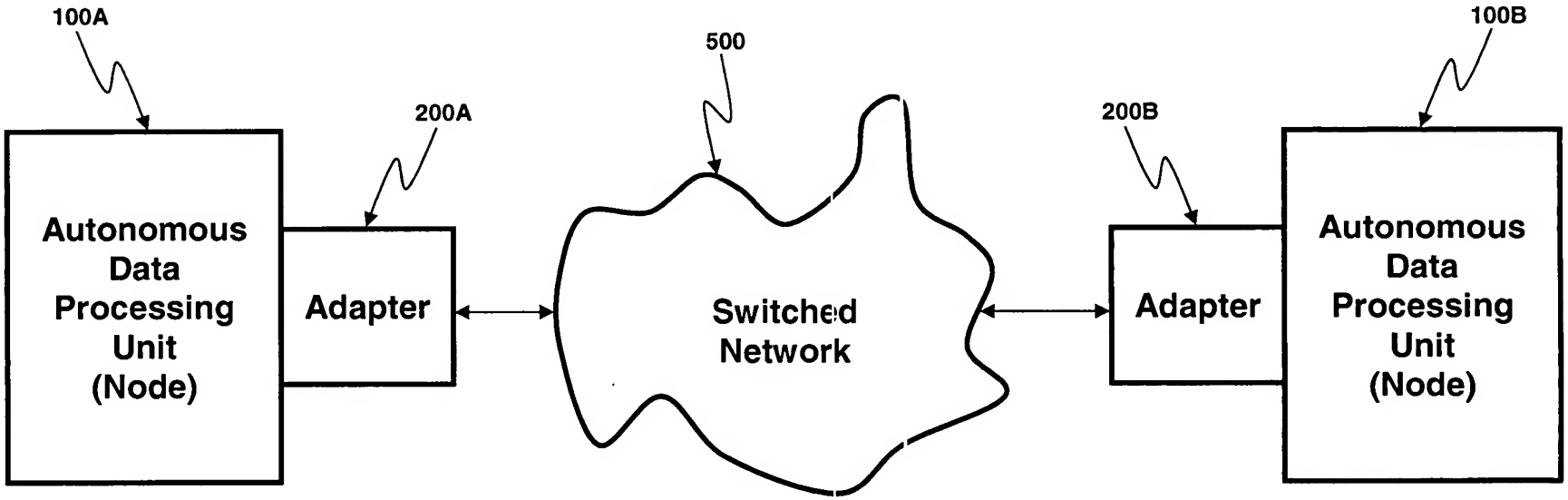

100A
200A
500
200B
100B
Autonomous Data Processing Unit (Node)
Adapter
Switched Network
Adapter
Autonomous Data Processing Unit (Node)

Figure 3

Send-Receive

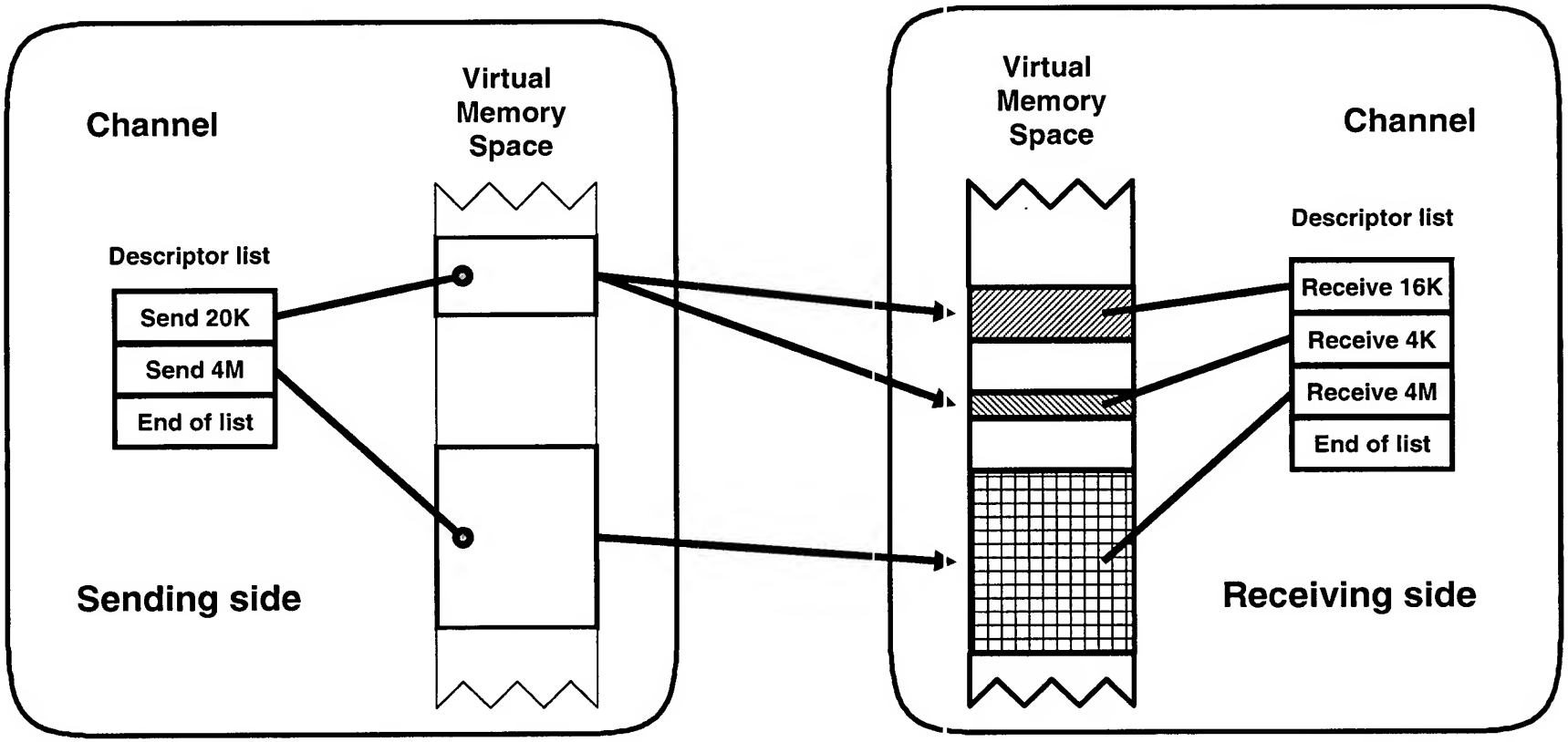


Figure 4

Remote Read-Write

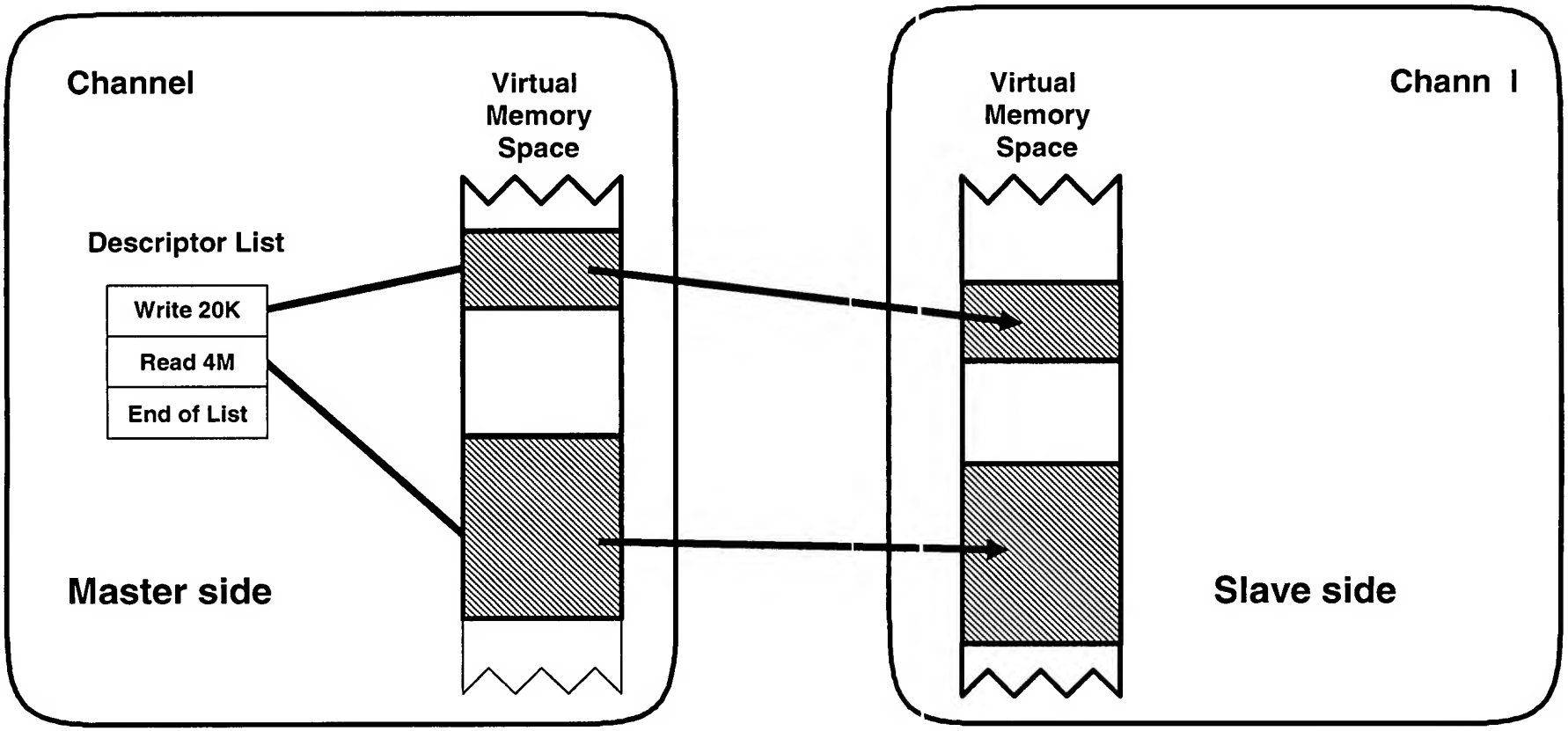


Figure 5

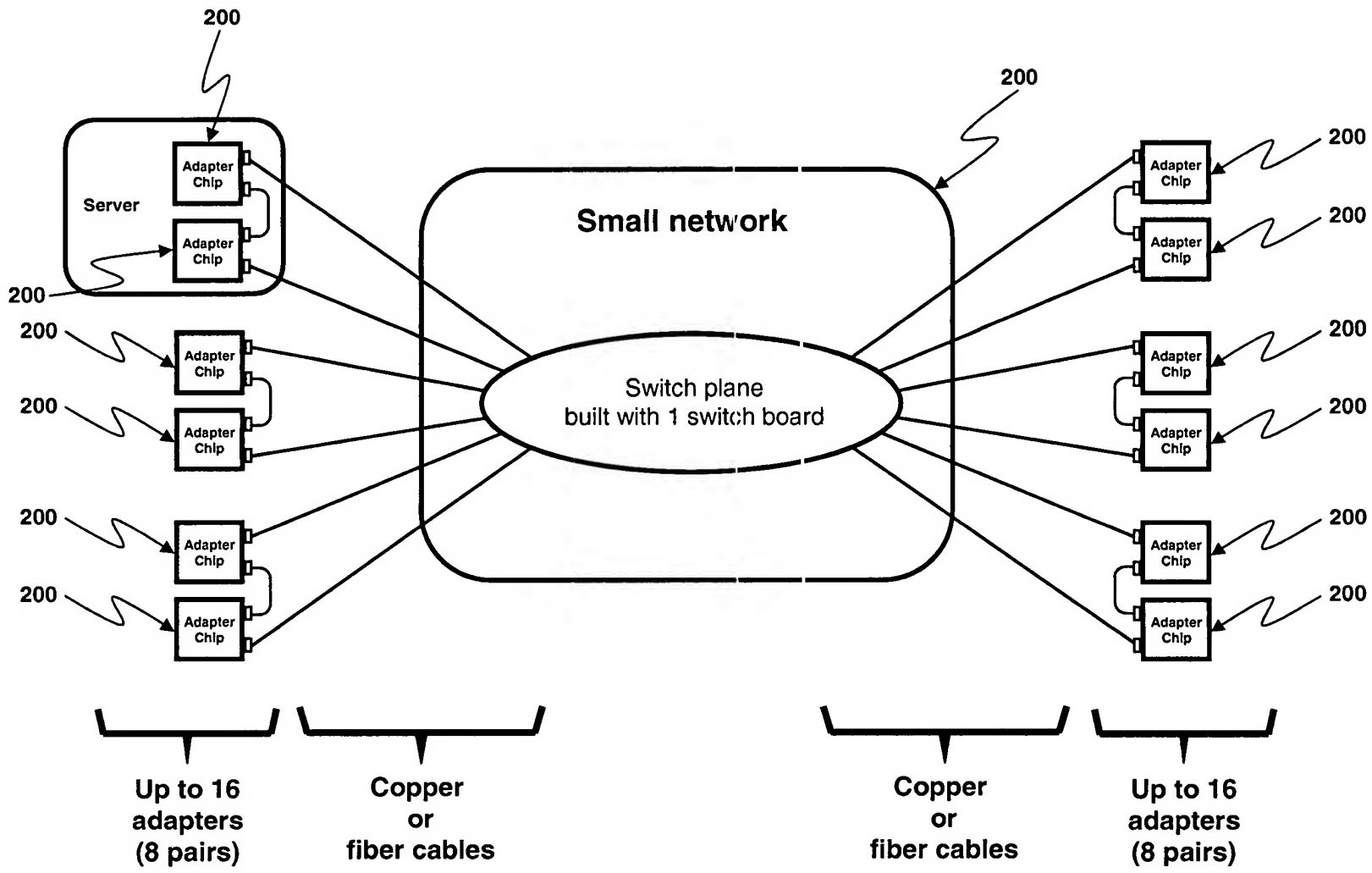

200
Server
Adapter Chip
Adapter Chip
200
Small network
Switch plane
built with 1 switch board
Up to 16 adapters (8 pairs)
Copper or fiber cables
Copper or fiber cables
Up to 16 adapters (8 pairs)

Figure 6

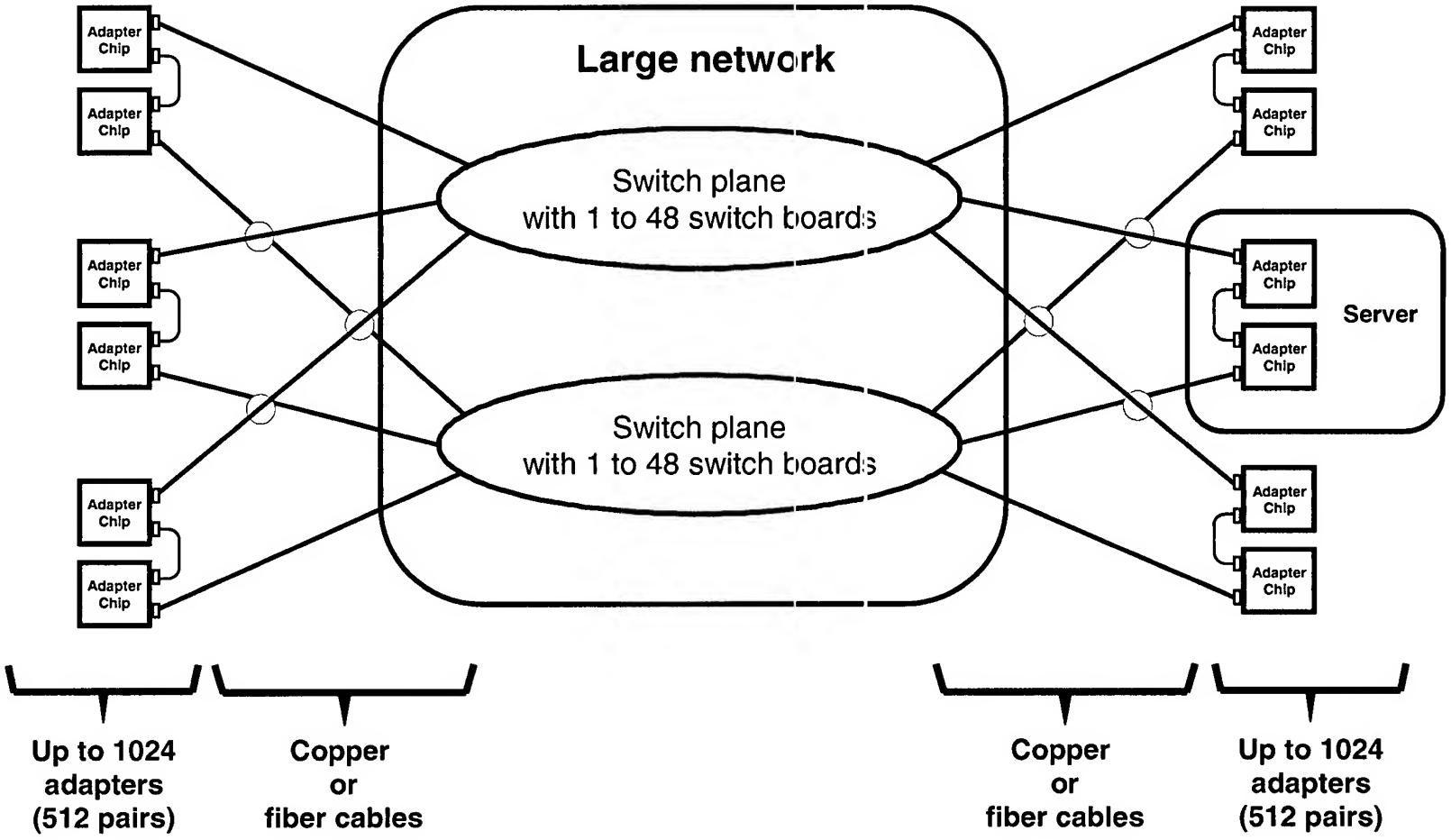

Large network
Switch plane
with 1 to 48 switch boards
Switch plane
with 1 to 48 switch boards
Adapter Chip
Server
Up to 1024 adapters (512 pairs)
Copper or fiber cables
Copper or fiber cables
Up to 1024 adapters (512 pairs)

Figure 7

Programming Interface

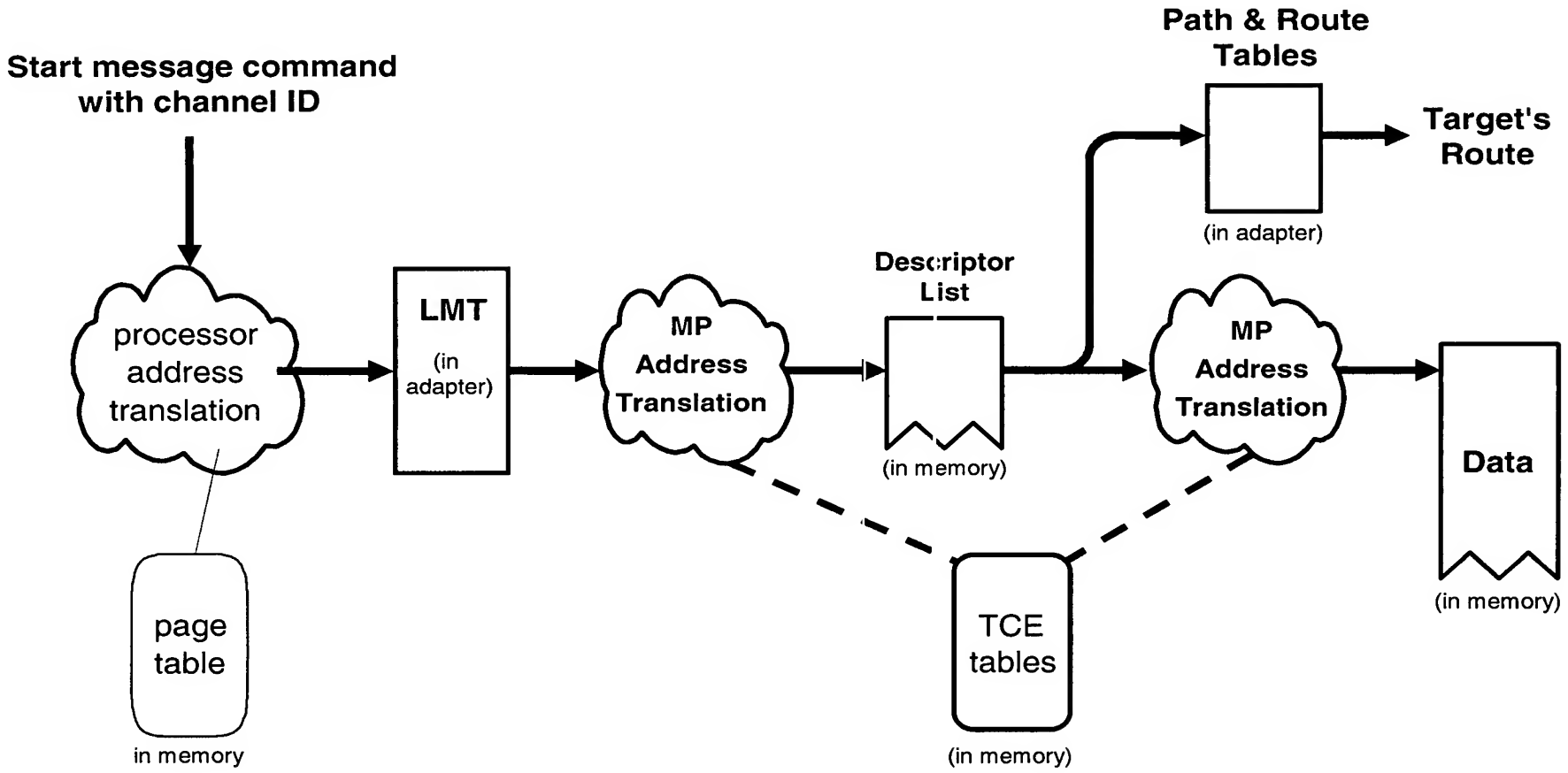


Figure 8

Address Translation

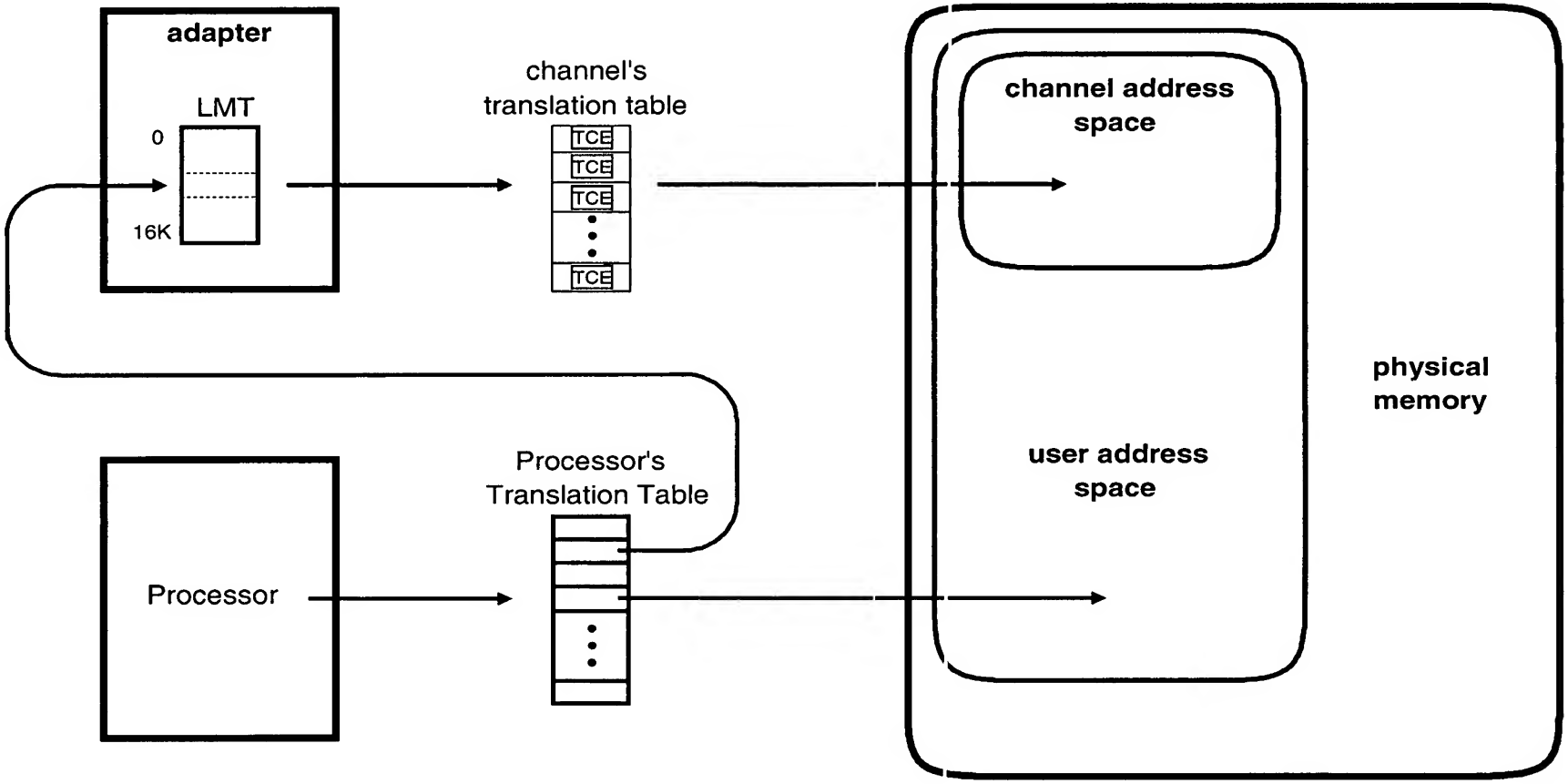


Figure 9

Address Translation with 4K pages

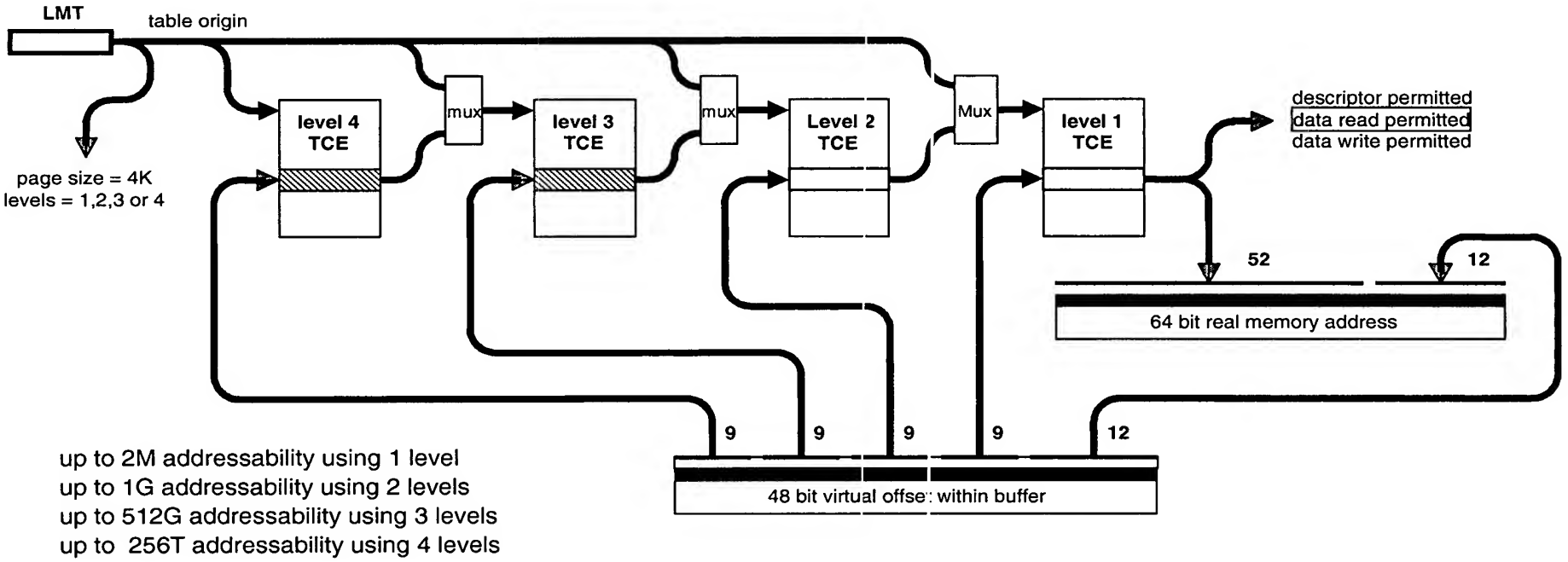
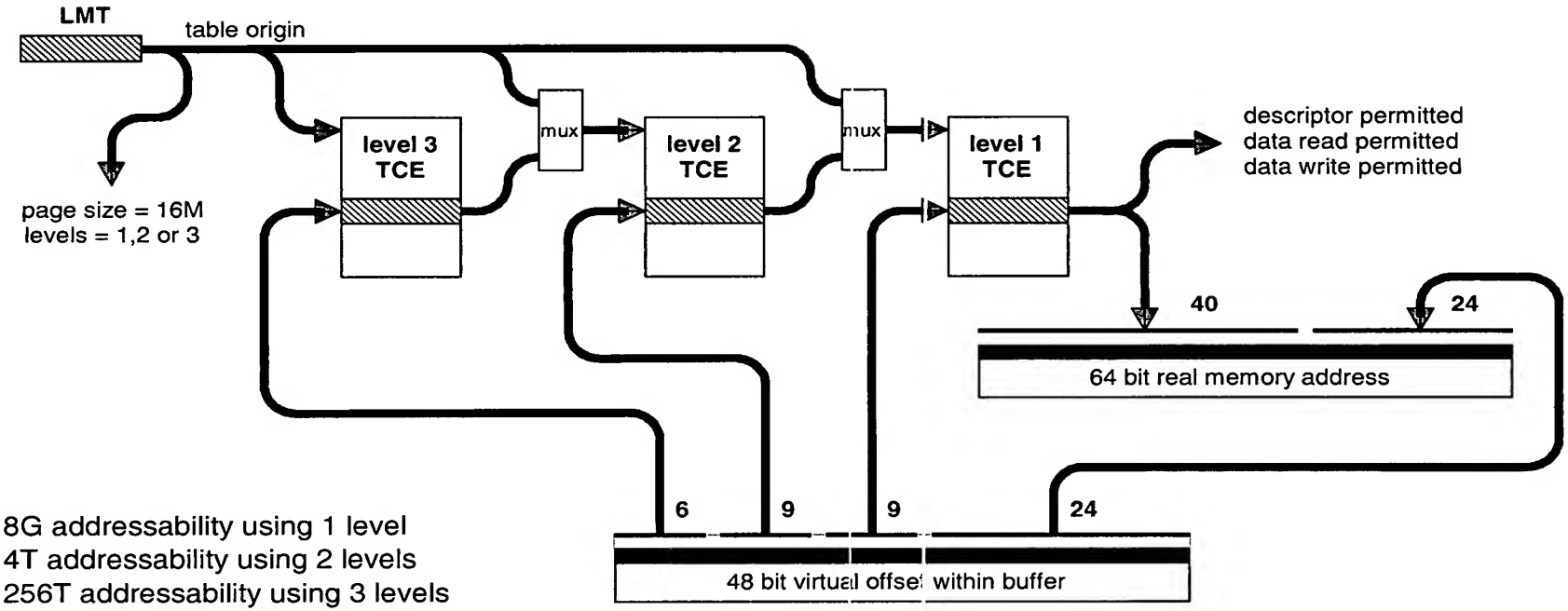


Figure 10

Address Translation with 16M pages



up to 8G addressability using 1 level
up to 4T addressability using 2 levels
up to 256T addressability using 3 levels

Figure 11

Adapter Identification

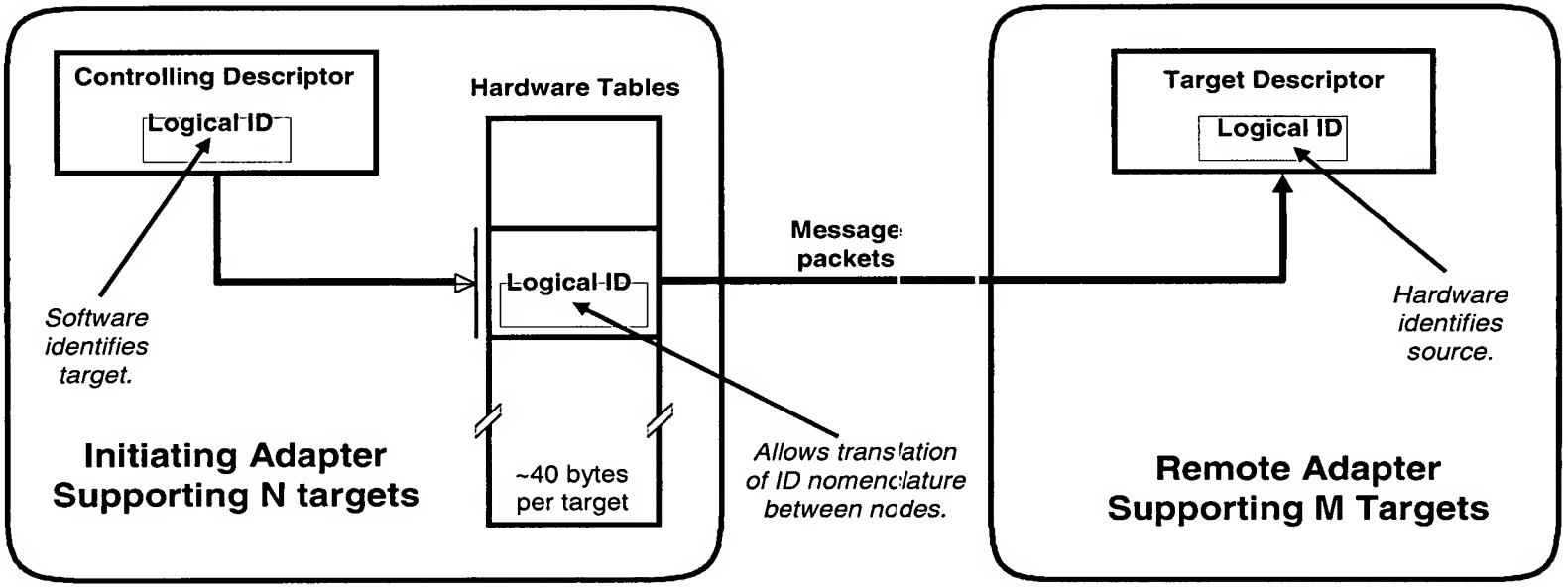


Figure 12

Broadcast Function

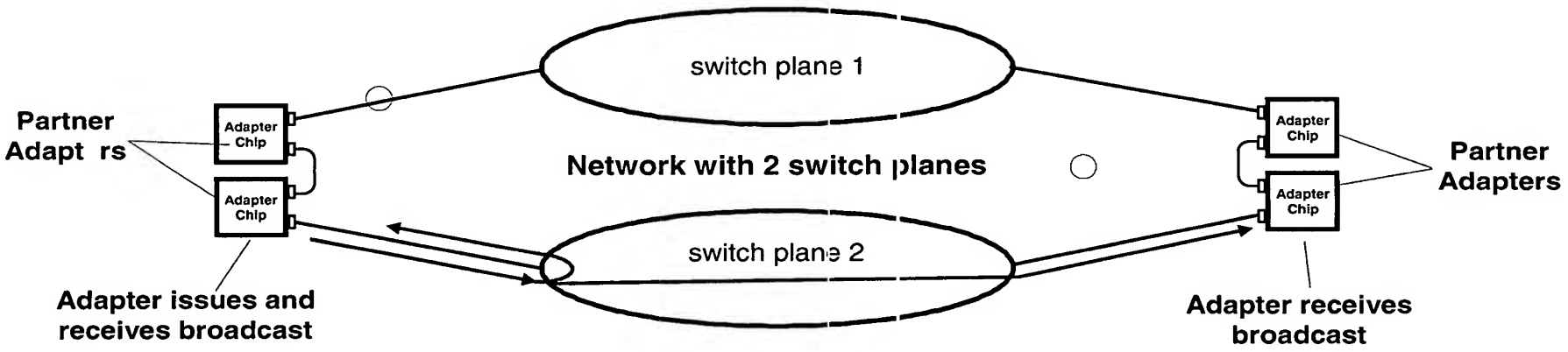


Figure 13

Processor Interrupts

Channel Interrupt Generation

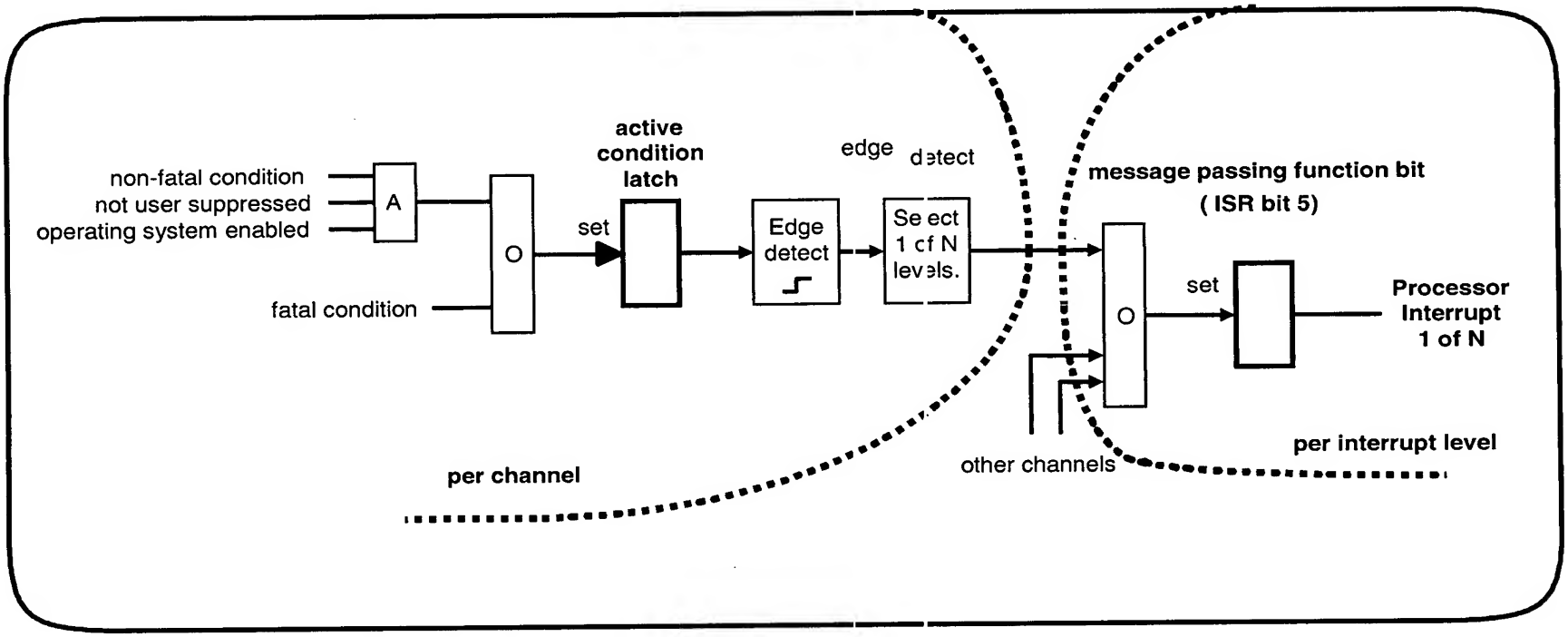


Figure 14

Defined Address Fields

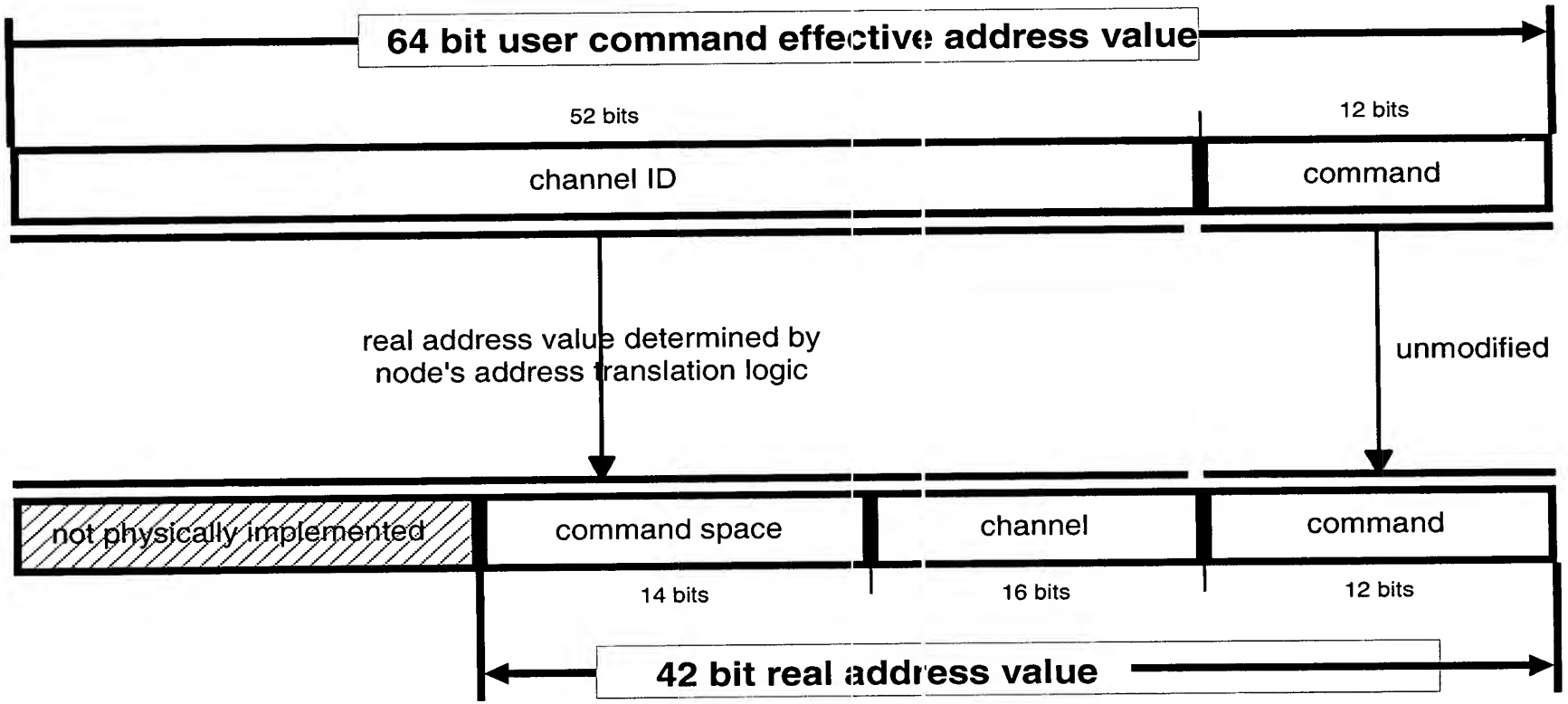


Figure 15

Channel States

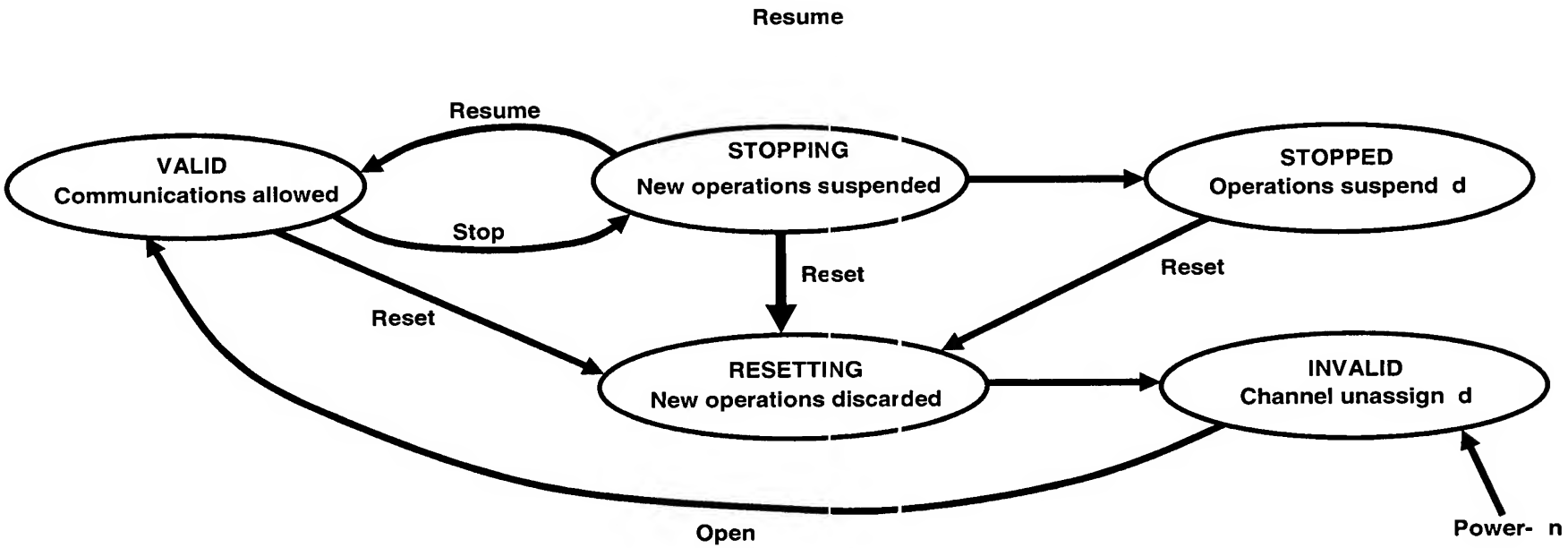


Figure 16

Local Mapping Table (LMT) Entries

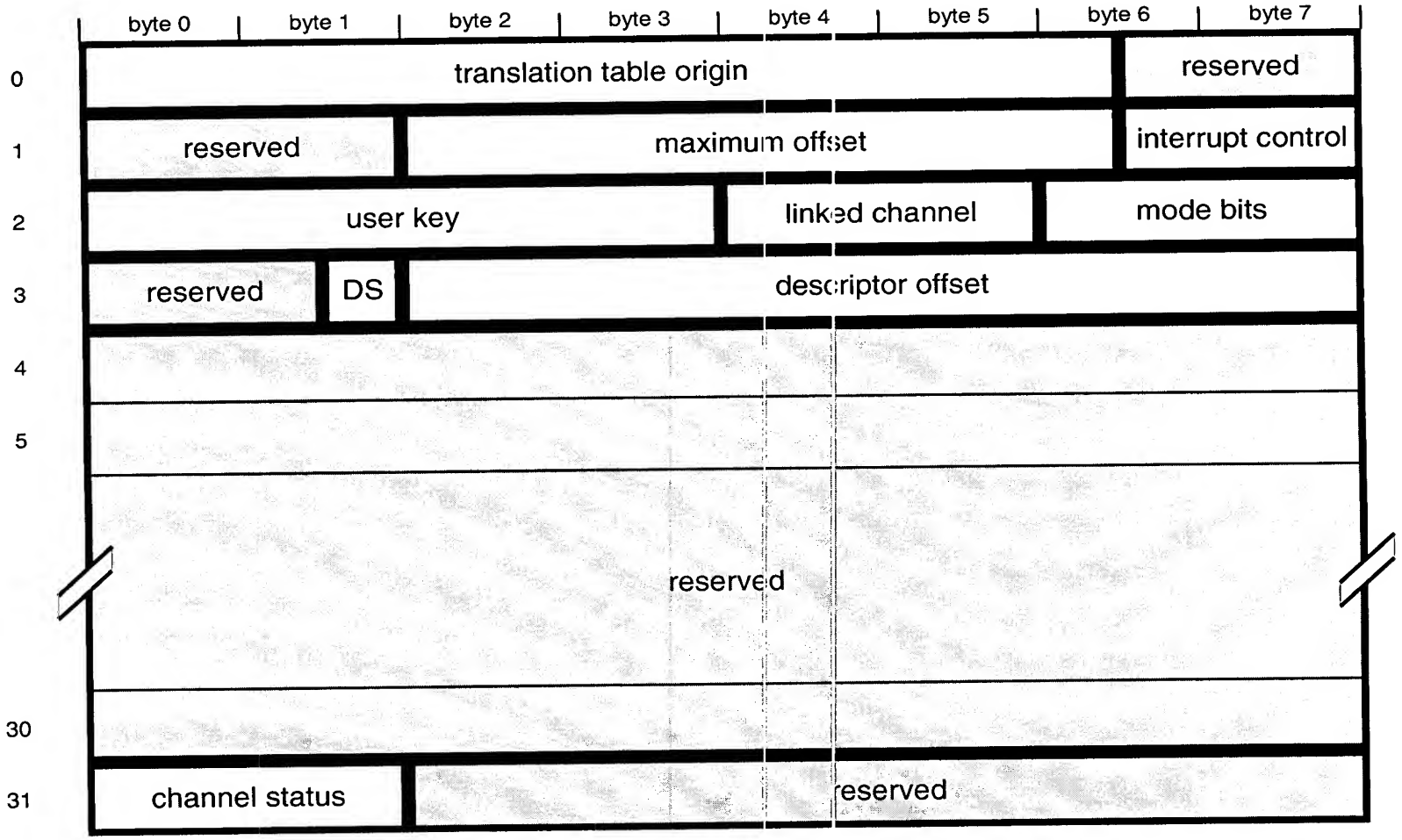


Figure 17

Translation Control Elements

TCE format

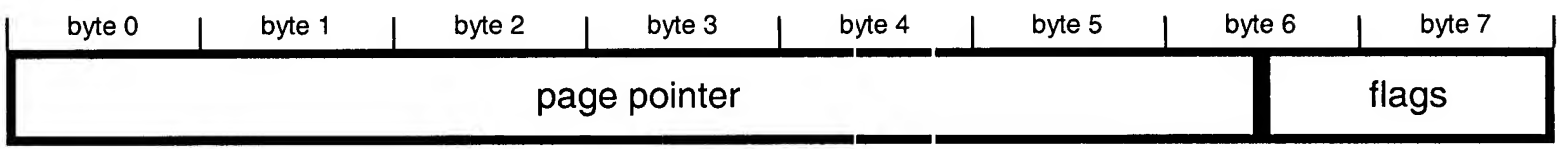


Figure 18

Remote Write

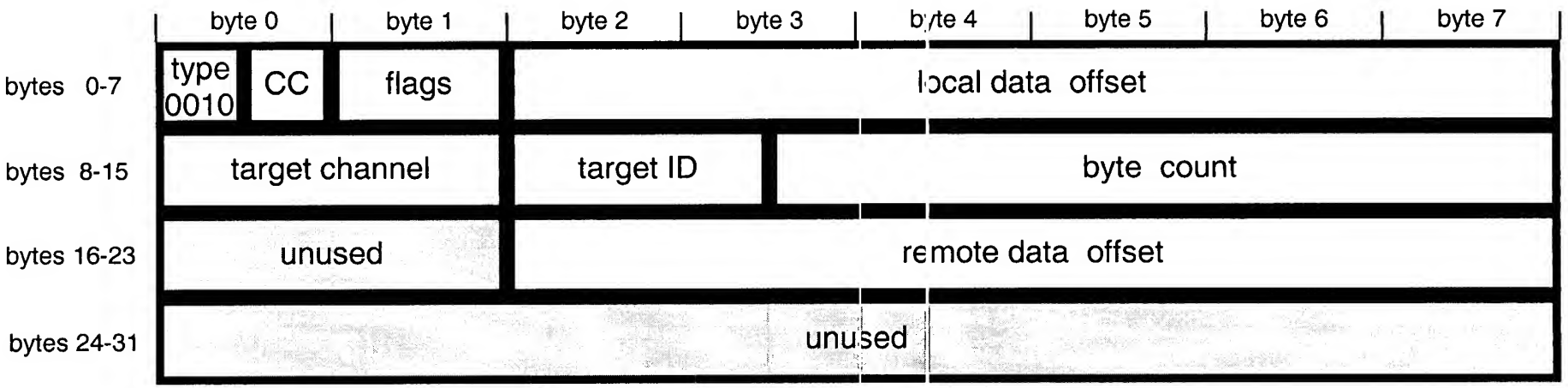


Figure 19

Remote Read

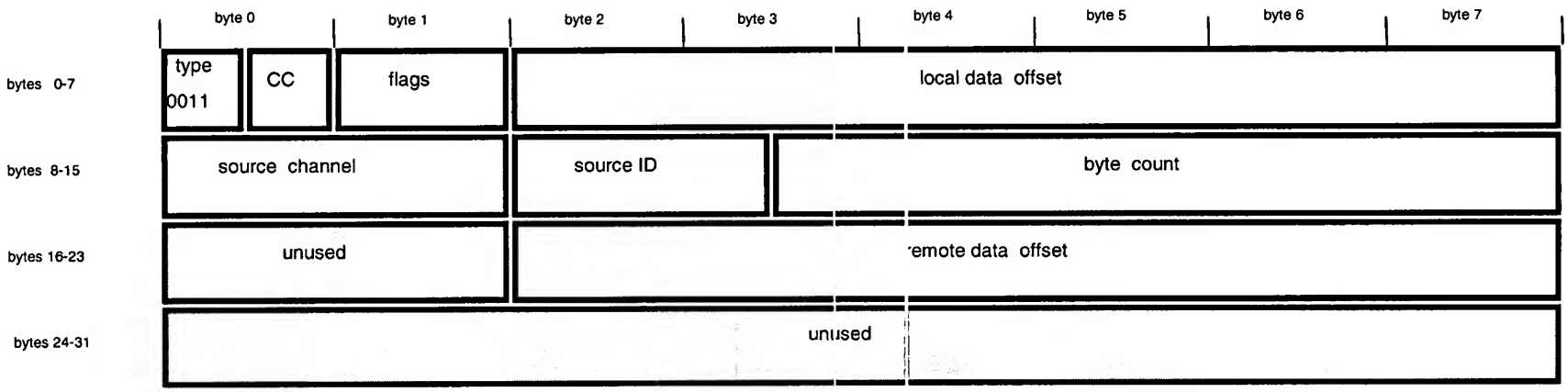


Figure 20

Source of Push

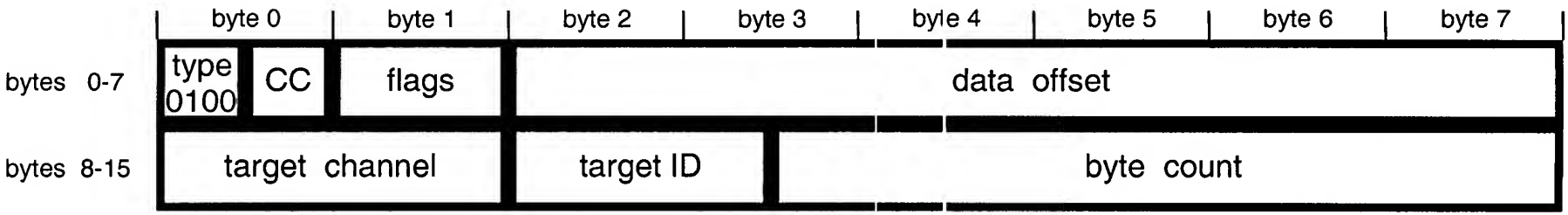


Figure 21

Target of push

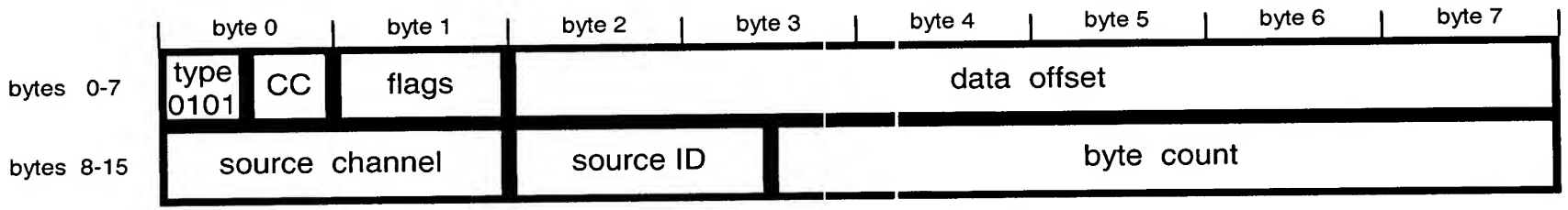


Figure 22

Source of Pull

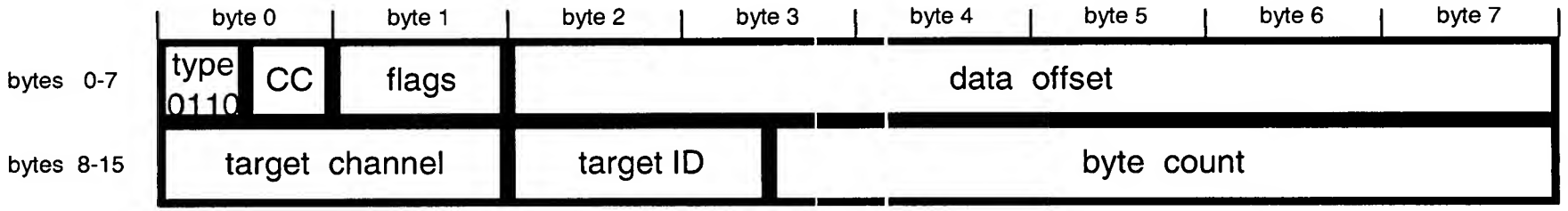


Figure 23

Target of pull

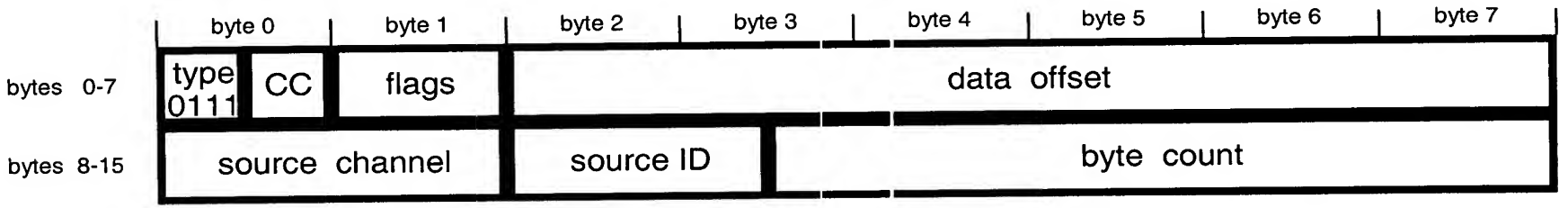


Figure 24

Preload data

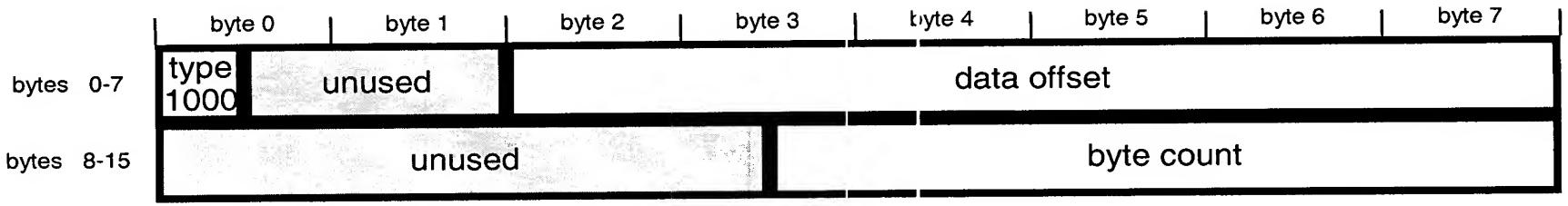


Figure 25

Branch

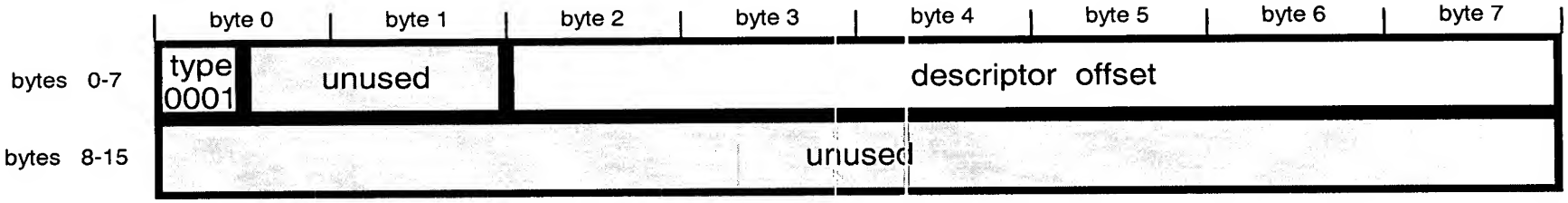


Figure 26

Path Table Entry

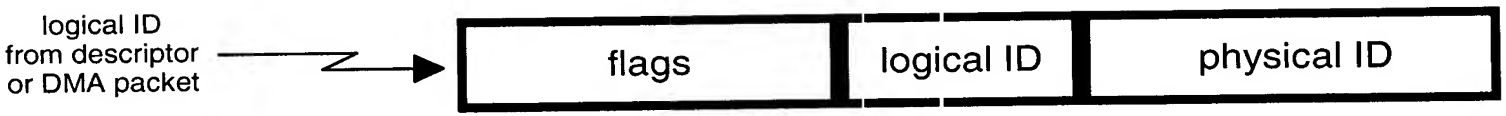


Figure 27

Route Table Entry

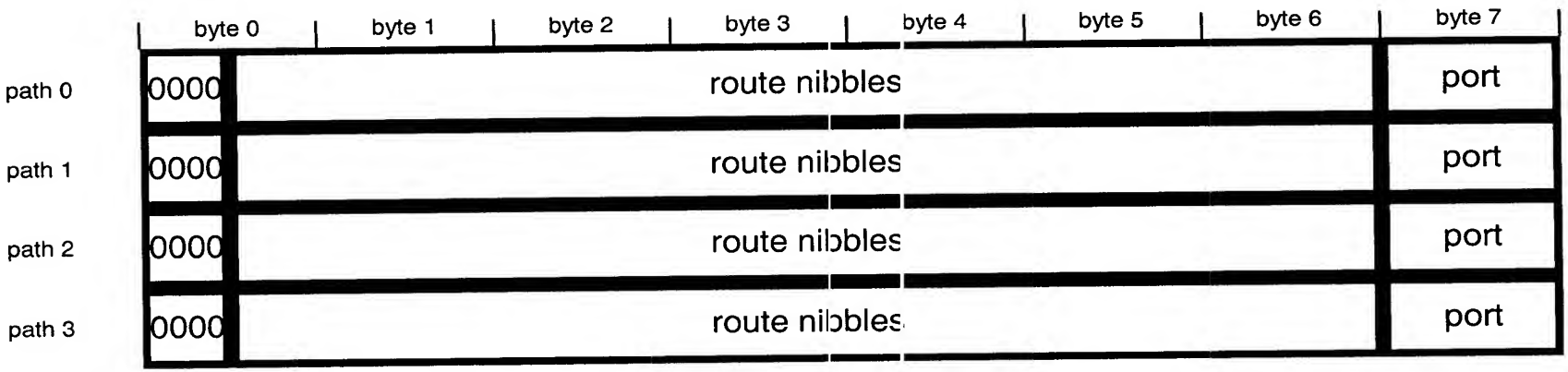


Figure 28

Broadcast Registers

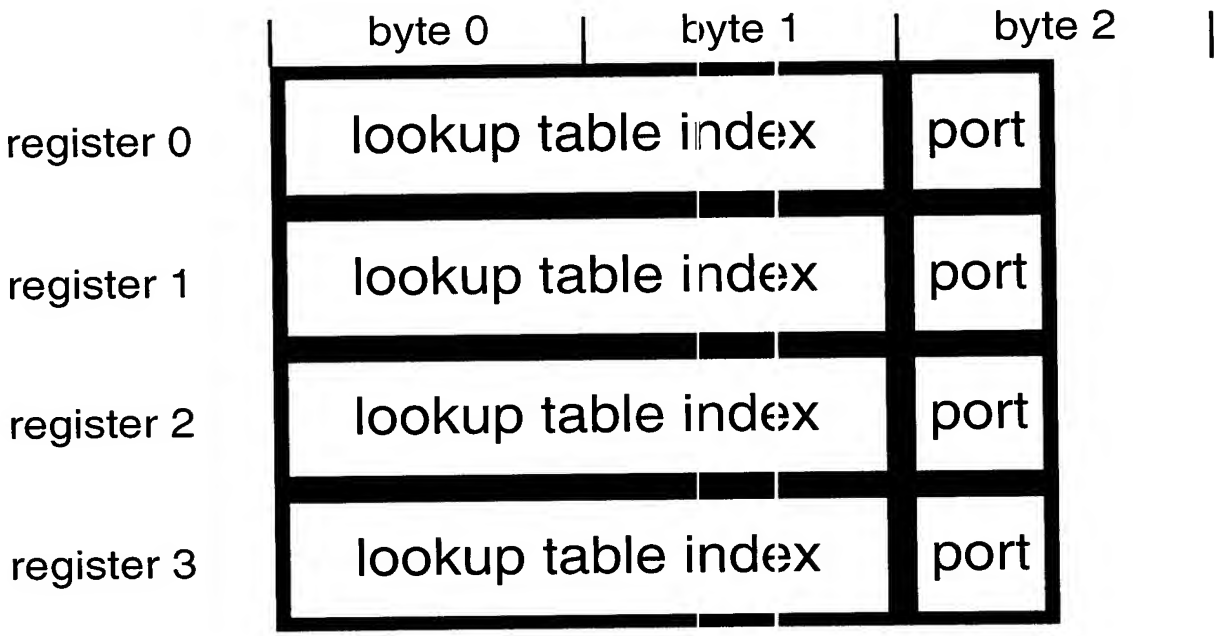


Figure 29

Sequence Table Entry

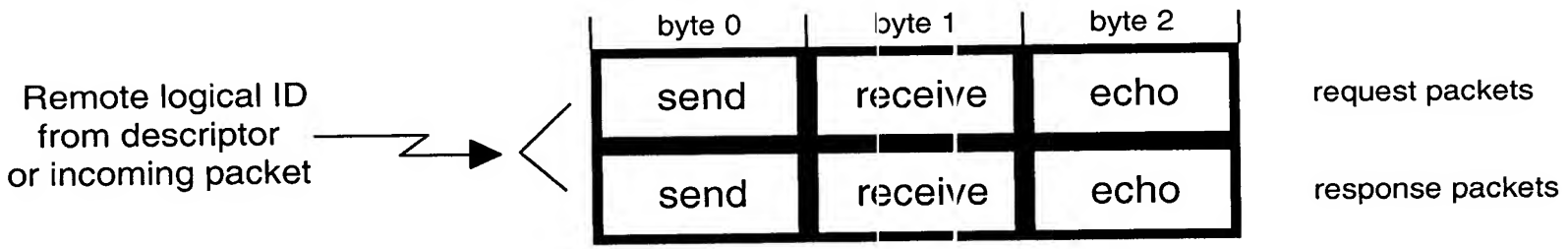


Figure 30

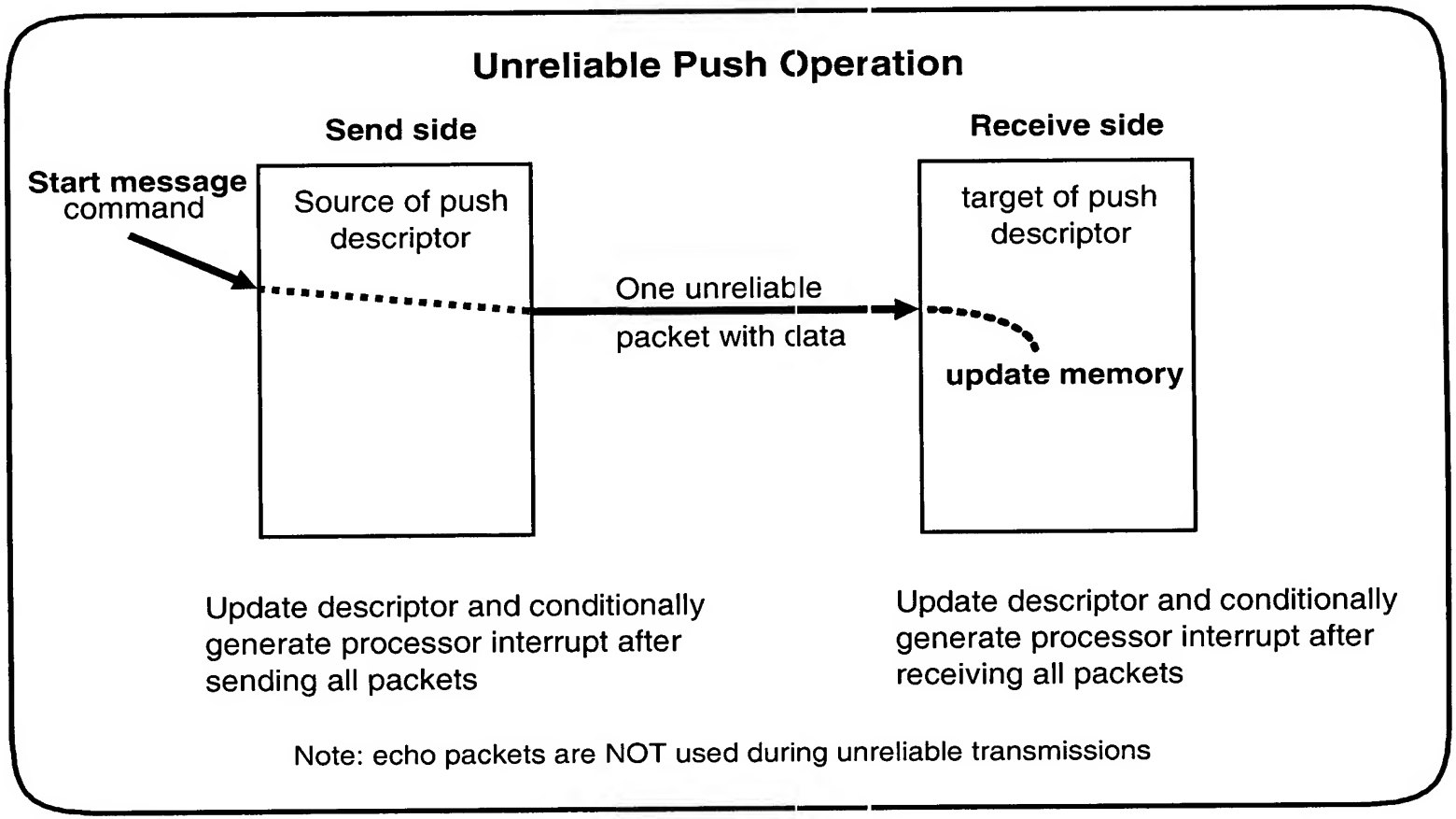

Unreliable Push Operation
Send side
Receive side
Start message command
Source of push descriptor
target of push descriptor
One unreliable packet with data
update memory
Update descriptor and conditionally generate processor interrupt after sending all packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
Note: echo packets are NOT used during unreliable transmissions

Figure 31

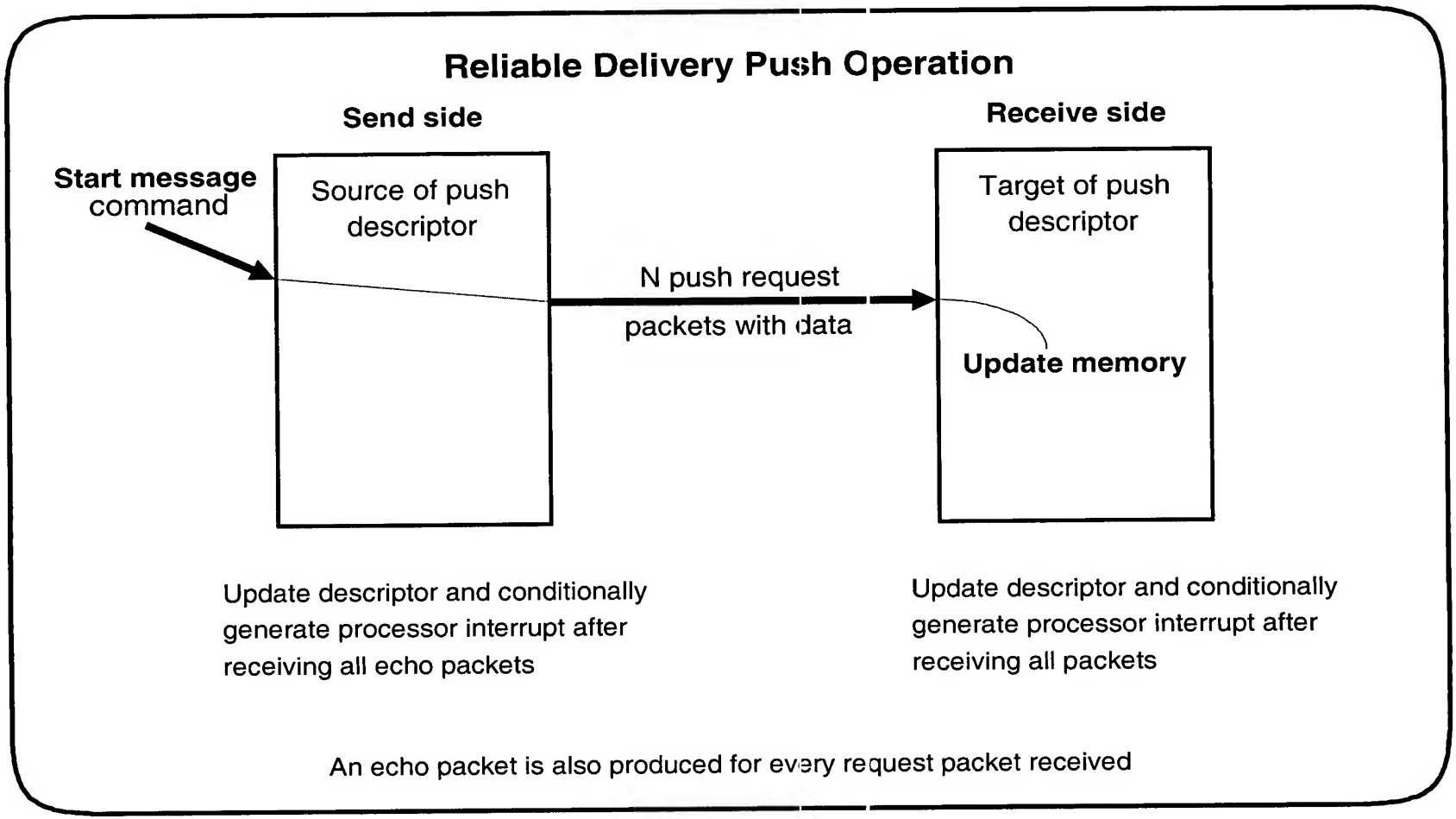

Reliable Delivery Push Operation
Send side
Receive side
Start message command
Source of push descriptor
Target of push descriptor
N push request packets with data
Update memory
Update descriptor and conditionally generate processor interrupt after receiving all echo packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
An echo packet is also produced for every request packet received

Figure 32

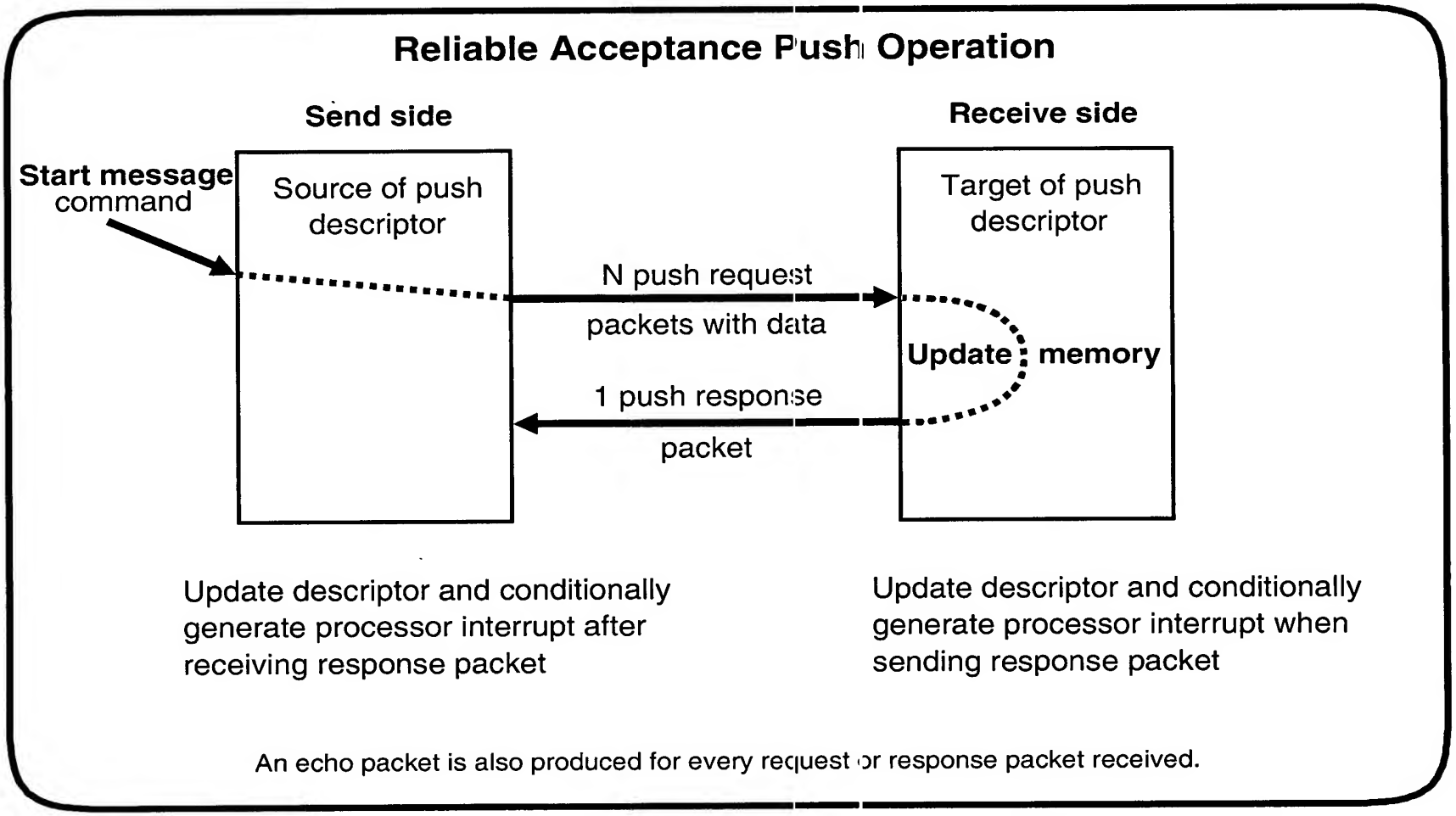

Reliable Acceptance Push Operation
Send side
Receive side
Start message command
Source of push descriptor
Target of push descriptor
N push request packets with data
Update memory
1 push response packet
Update descriptor and conditionally generate processor interrupt after receiving response packet
Update descriptor and conditionally generate processor interrupt when sending response packet
An echo packet is also produced for every request or response packet received.

Figure 33

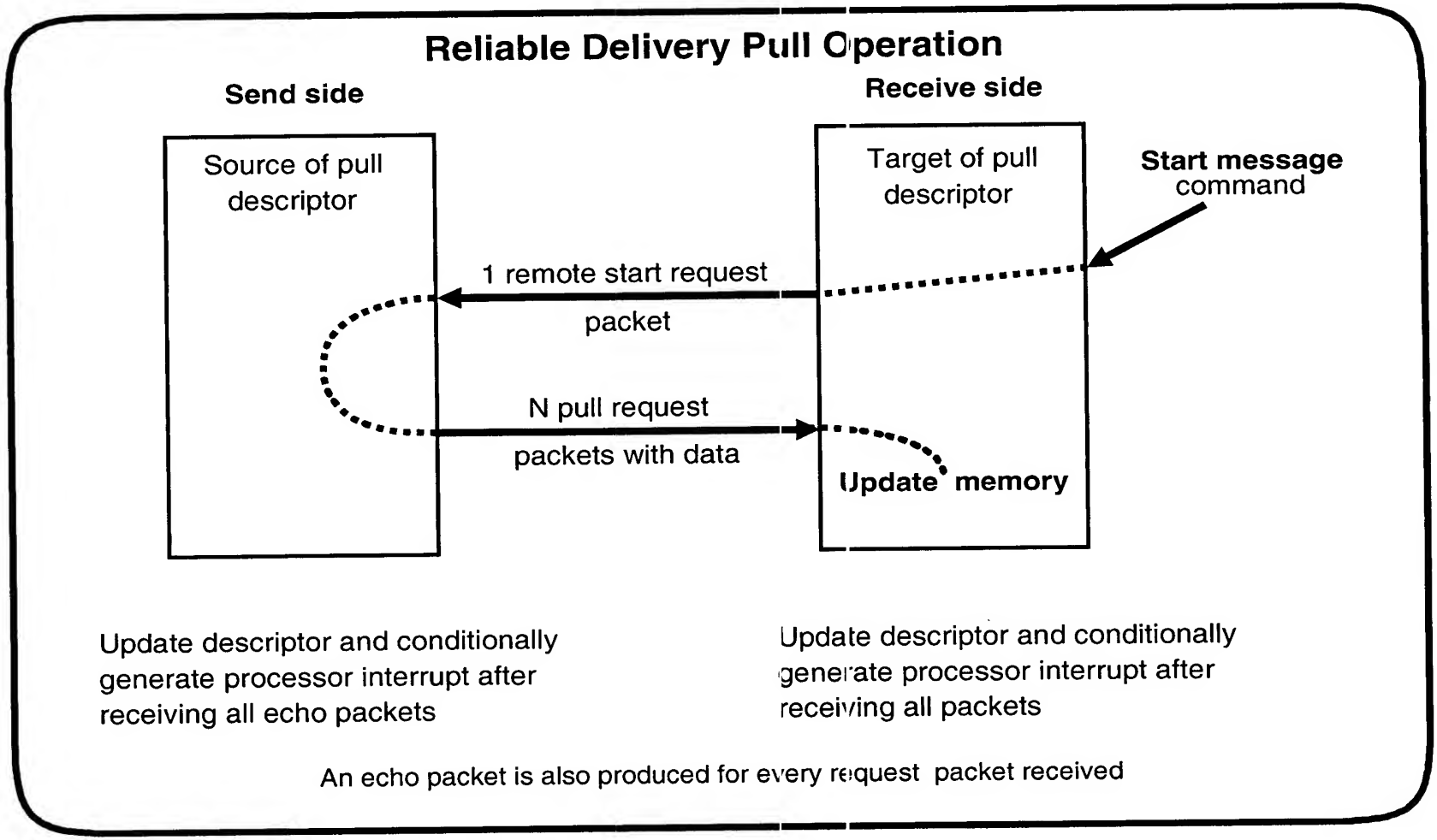

Reliable Delivery Pull Operation
Send side
Receive side
Source of pull descriptor
Target of pull descriptor
Start message command
1 remote start request packet
N pull request packets with data
Update memory
Update descriptor and conditionally generate processor interrupt after receiving all echo packets
Update descriptor and conditionally generate processor interrupt after receiving all packets
An echo packet is also produced for every request packet received

Figure 34

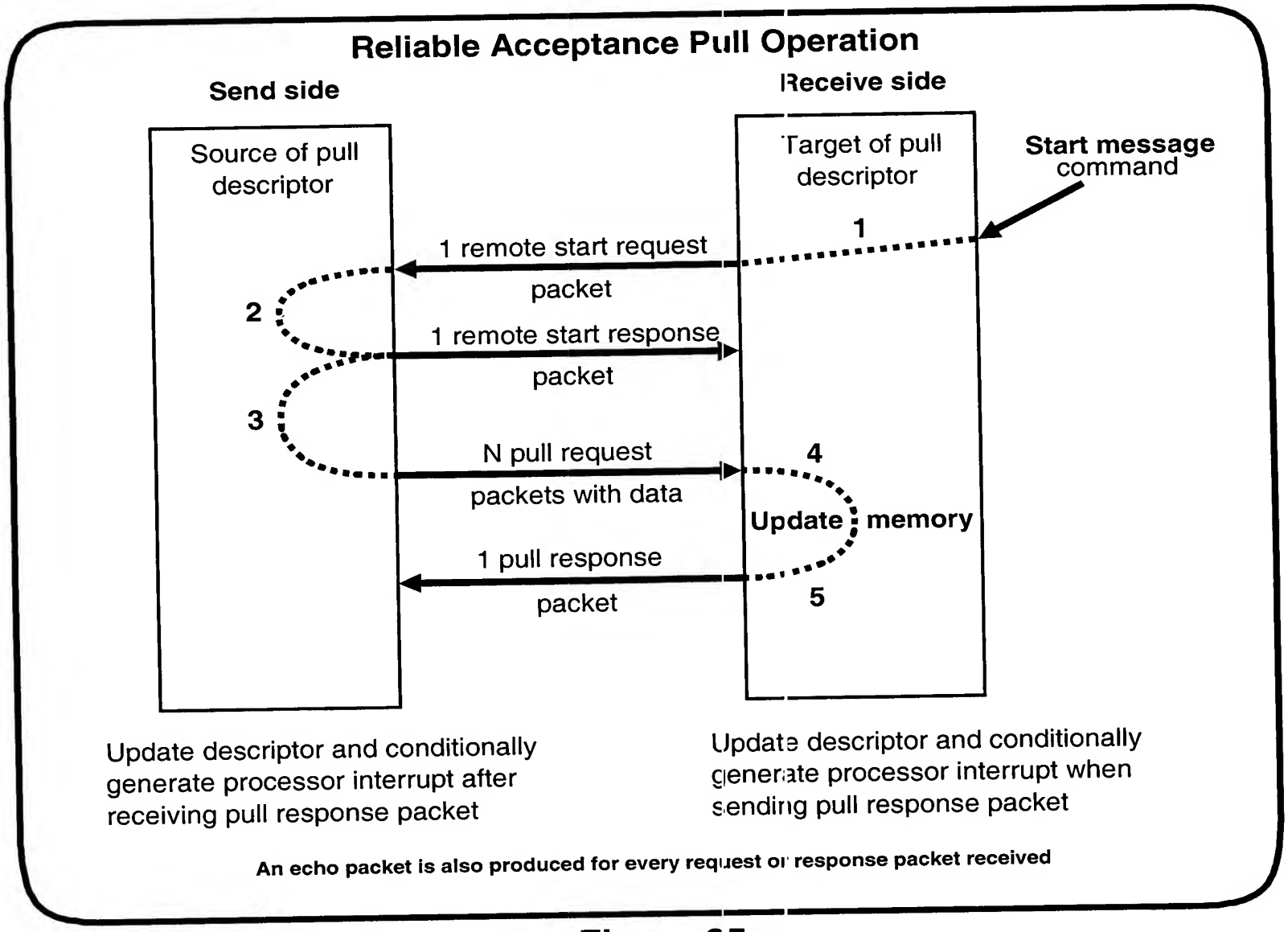

Reliable Acceptance Pull Operation
Send side
Receive side
Source of pull descriptor
Target of pull descriptor
Start message command
1
1 remote start request packet
2
1 remote start response packet
3
N pull request packets with data
4
Update memory
1 pull response packet
5
Update descriptor and conditionally generate processor interrupt after receiving pull response packet
Update descriptor and conditionally generate processor interrupt when sending pull response packet
An echo packet is also produced for every request or response packet received

Figure 35

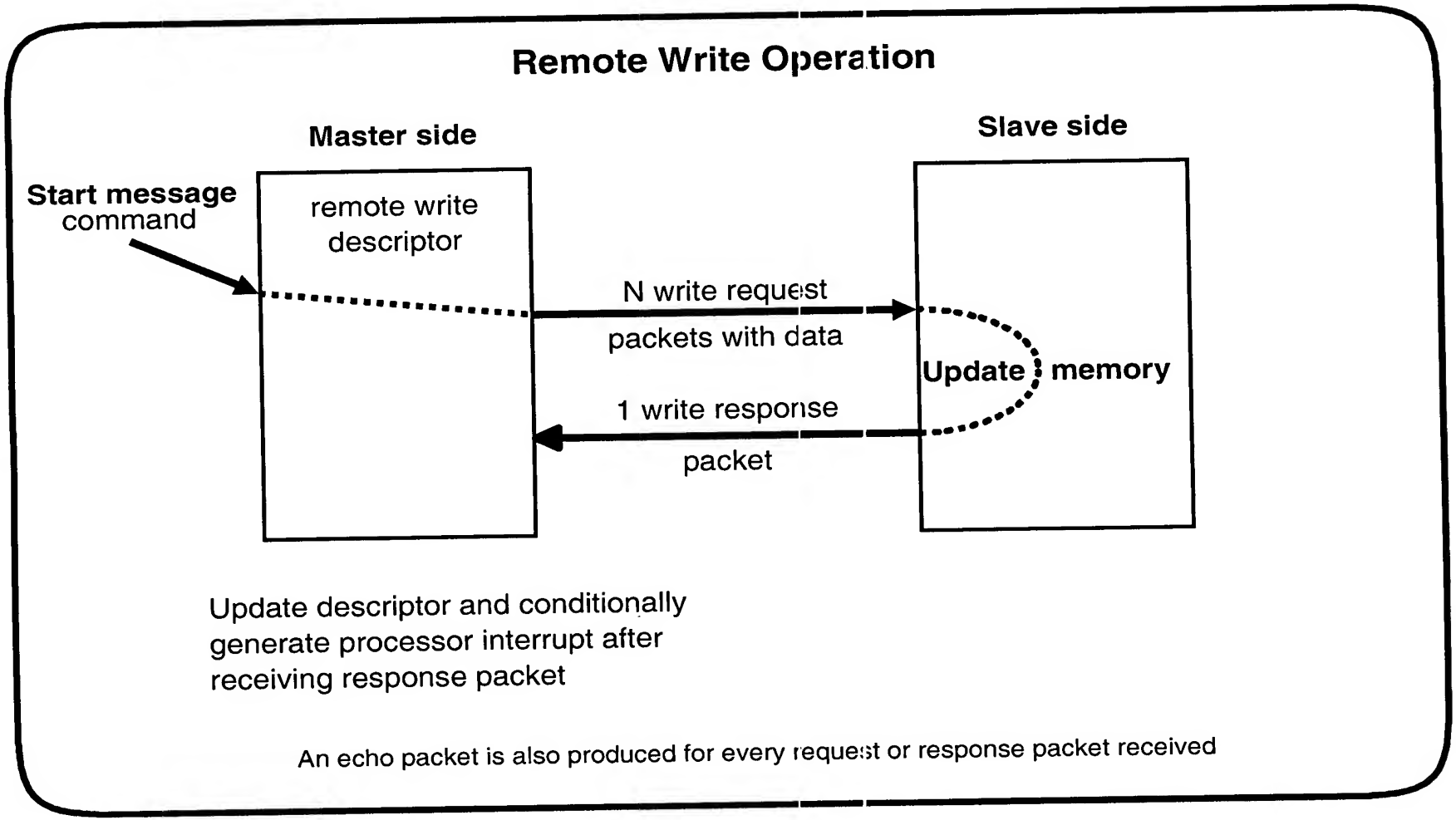

Remote Write Operation
Master side
Slave side
Start message
command
remote write
descriptor
N write request
packets with data
Update
memory
1 write response
packet
Update descriptor and conditionally
generate processor interrupt after
receiving response packet
An echo packet is also produced for every request or response packet received

Figure 36

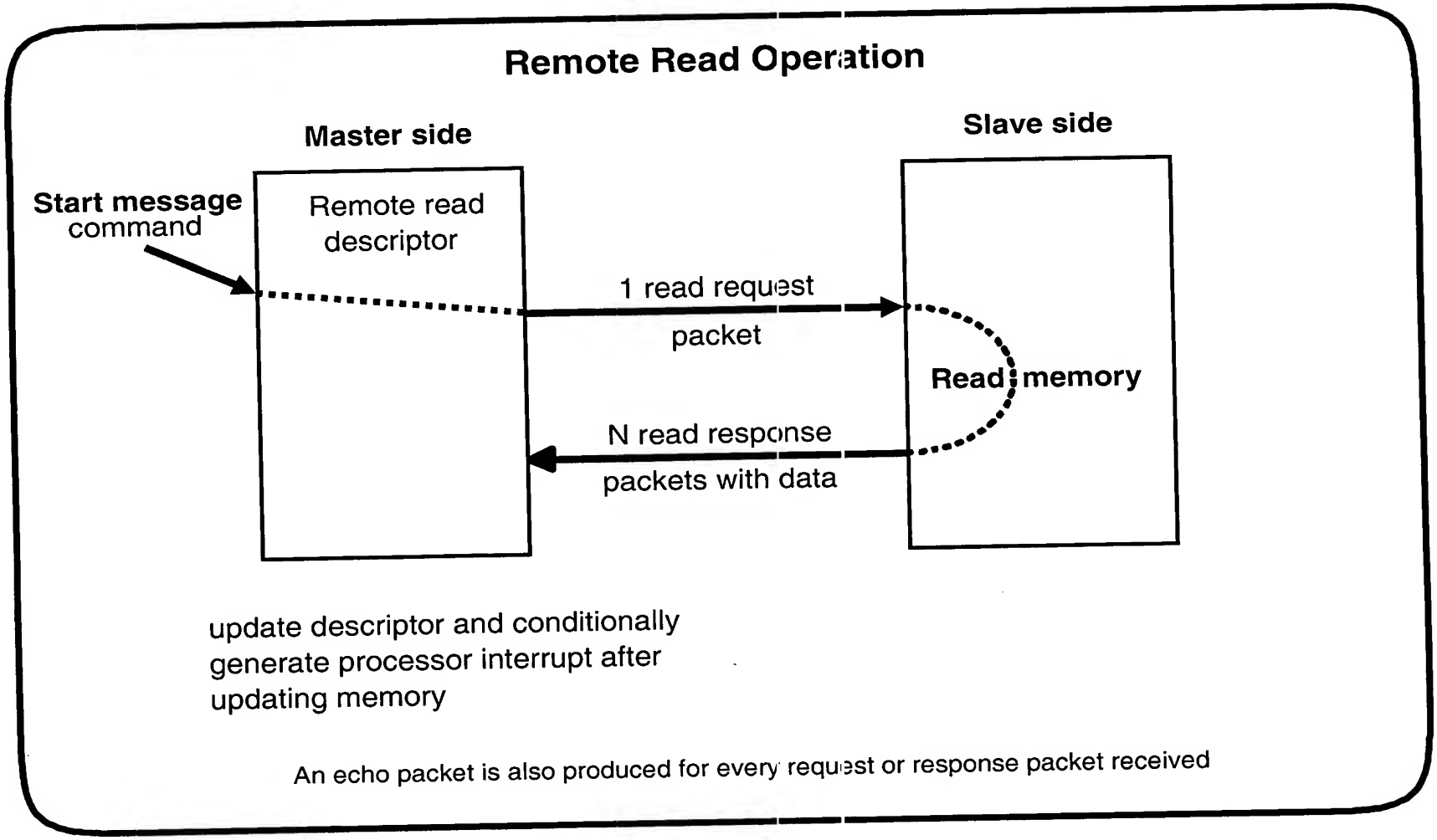

Remote Read Operation
Master side
Slave side
Start message command
Remote read descriptor
1 read request packet
Read memory
N read response packets with data
update descriptor and conditionally generate processor interrupt after updating memory
An echo packet is also produced for every request or response packet received

Figure 37

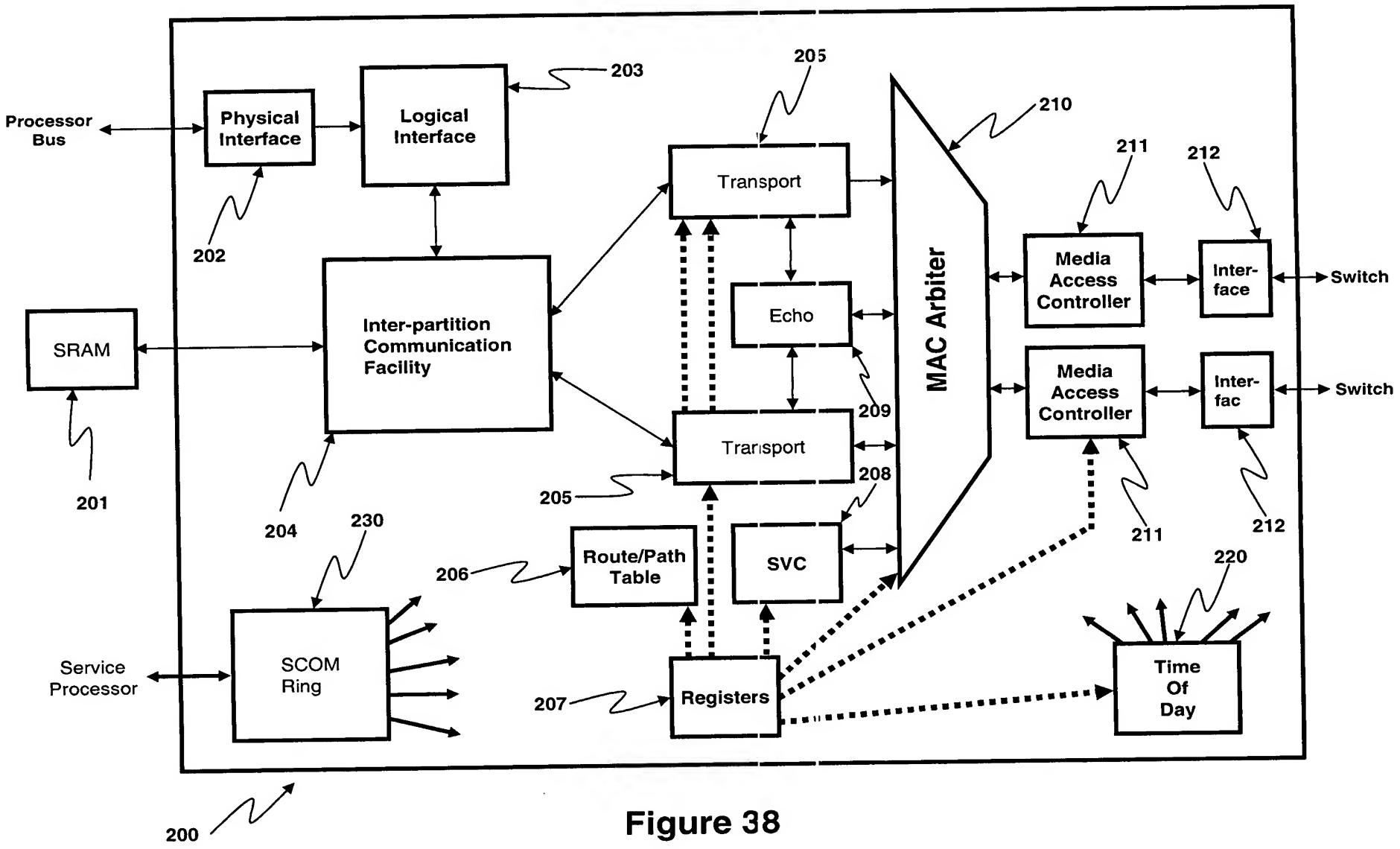

Processor Bus
Physical Interface
Logical Interface
203
205
210
211
212
202
Transport
Media Access Controller
Inter-face
Switch
SRAM
Inter-partition Communication Facility
Echo
MAC Arbiter
209
Media Access Controller
Inter-fac
Switch
201
204
Transport
205
208
211
212
230
206
Route/Path Table
SVC
220
Service Processor
SCOM Ring
207
Registers
Time Of Day
200

Figure 38

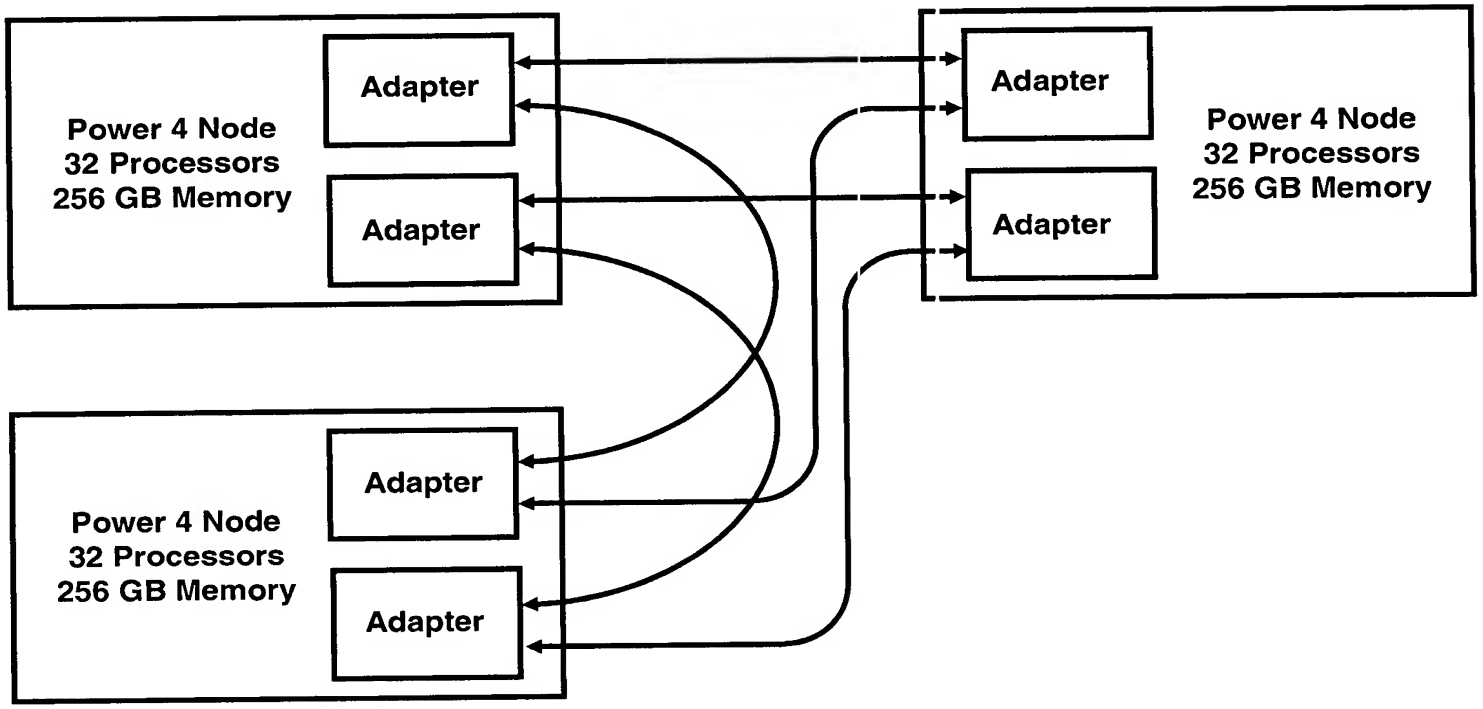

Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter
Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter
Power 4 Node
32 Processors
256 GB Memory
Adapter
Adapter

Figure 39

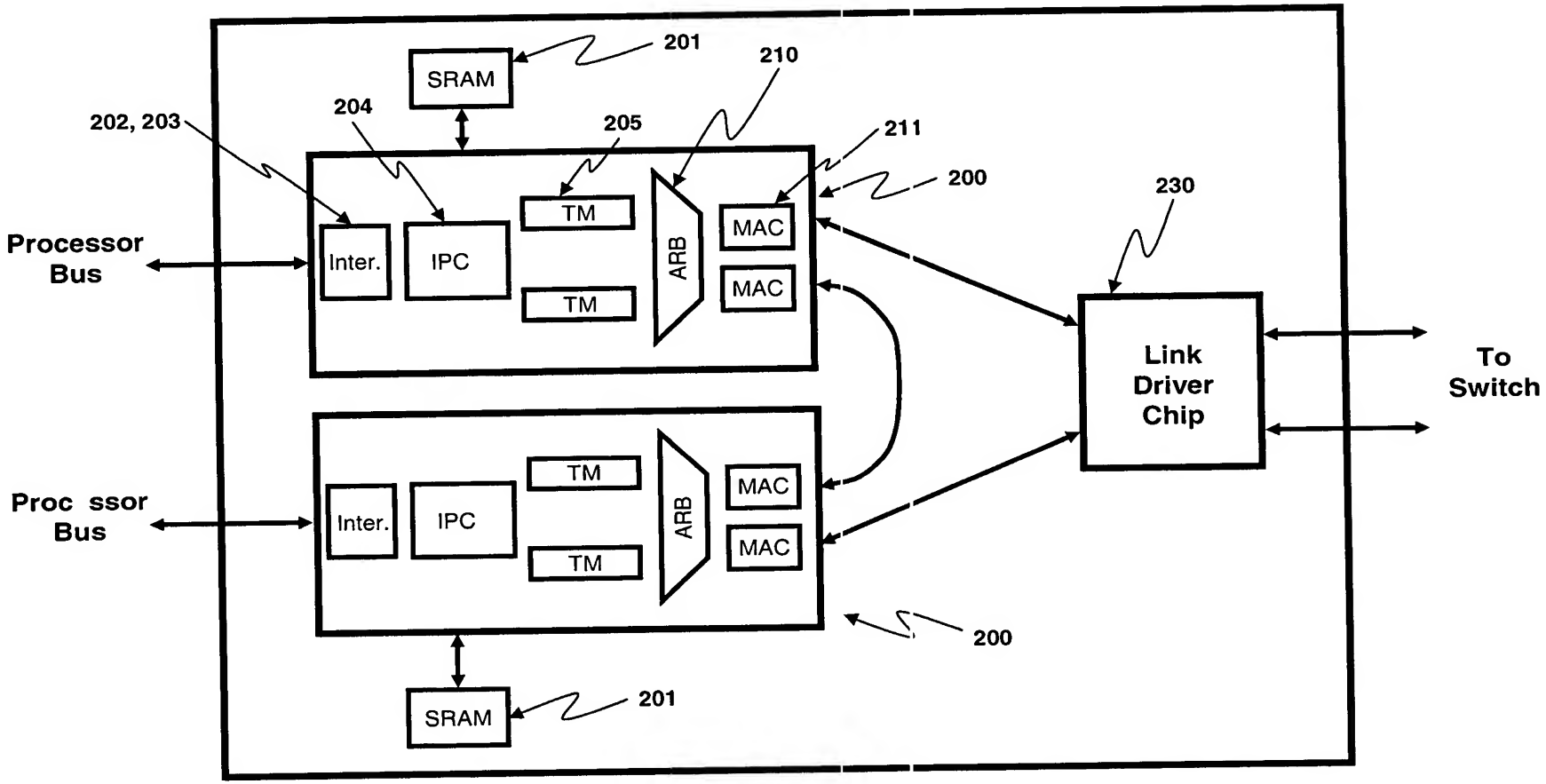

SRAM
201
210
204
202, 203
205
211
200
230
Processor Bus
Inter.
IPC
TM
TM
ARB
MAC
MAC
Link Driver Chip
To Switch
Proc ssor Bus
Inter.
IPC
TM
TM
ARB
MAC
MAC
200
SRAM
201

Figure 40

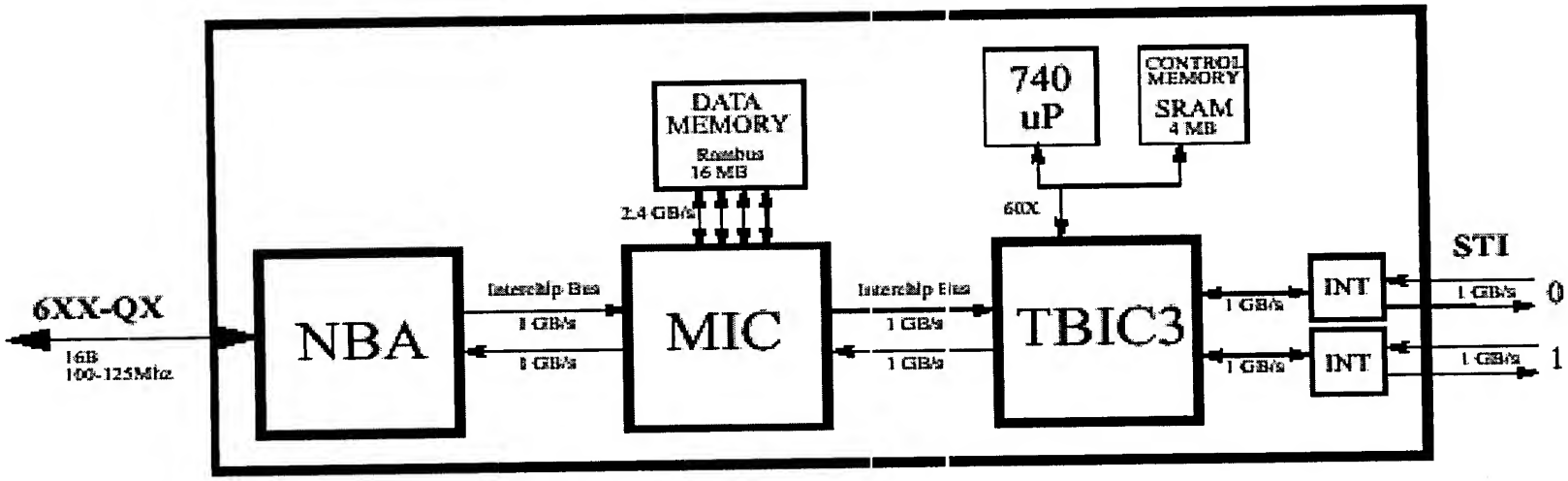


FIGURE 10. Colony Adapter

From page 32 of the spec – inclusion speculative

Figure 41

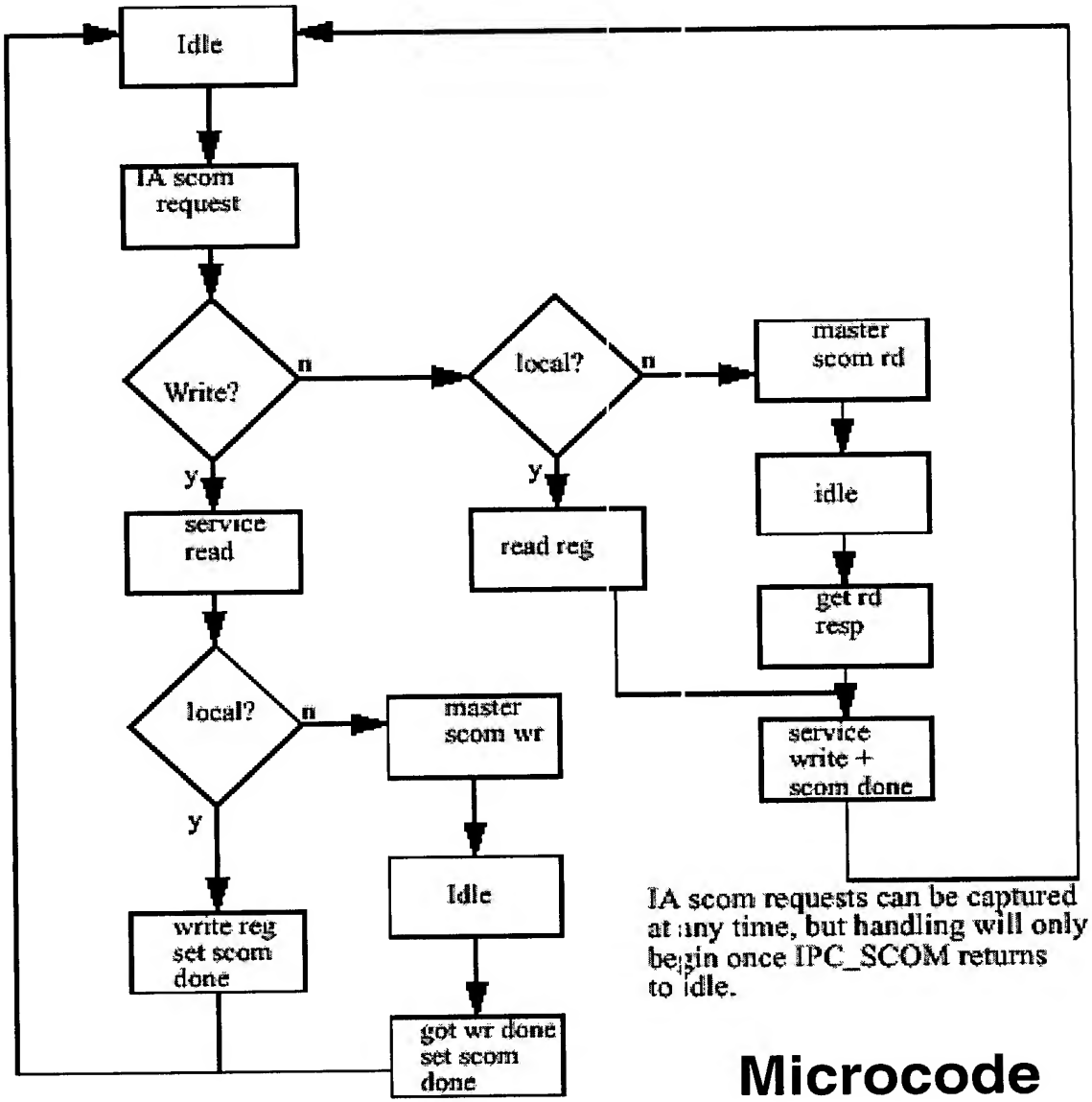

Idle
IA scom request
Write?
n
y
local?
n
y
master scom rd
idle
get rd resp
service write + scom done
read reg
service read
local?
n
y
master scom wr
Idle
got wr done set scom done
write reg set scom done
IA scom requests can be captured at any time, but handling will only begin once IPC_SCOM returns to idle.
Microcode

Figure 42

AUTO TRACKING OF BAD PATHS

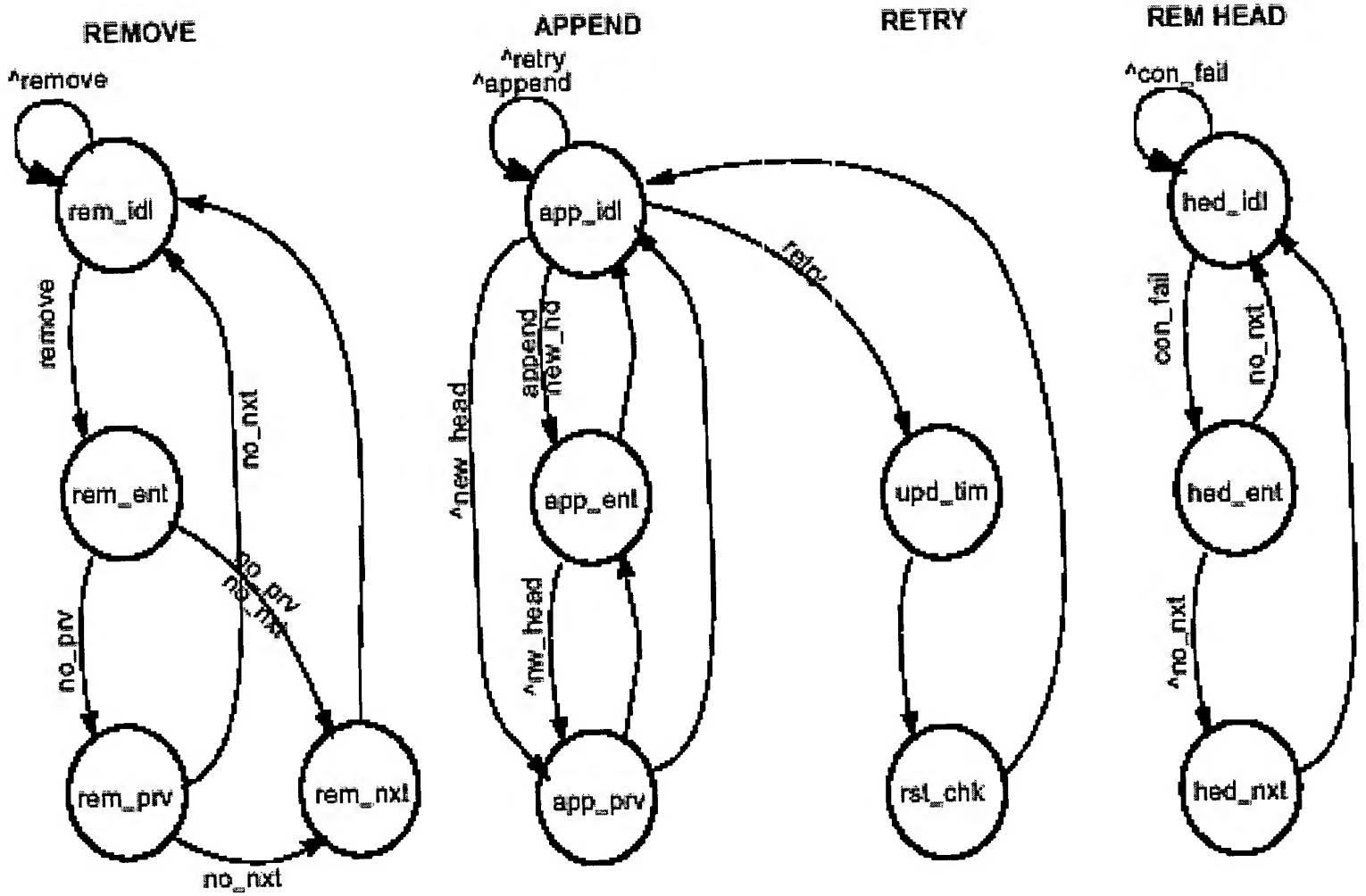


Figure 43

Formatter

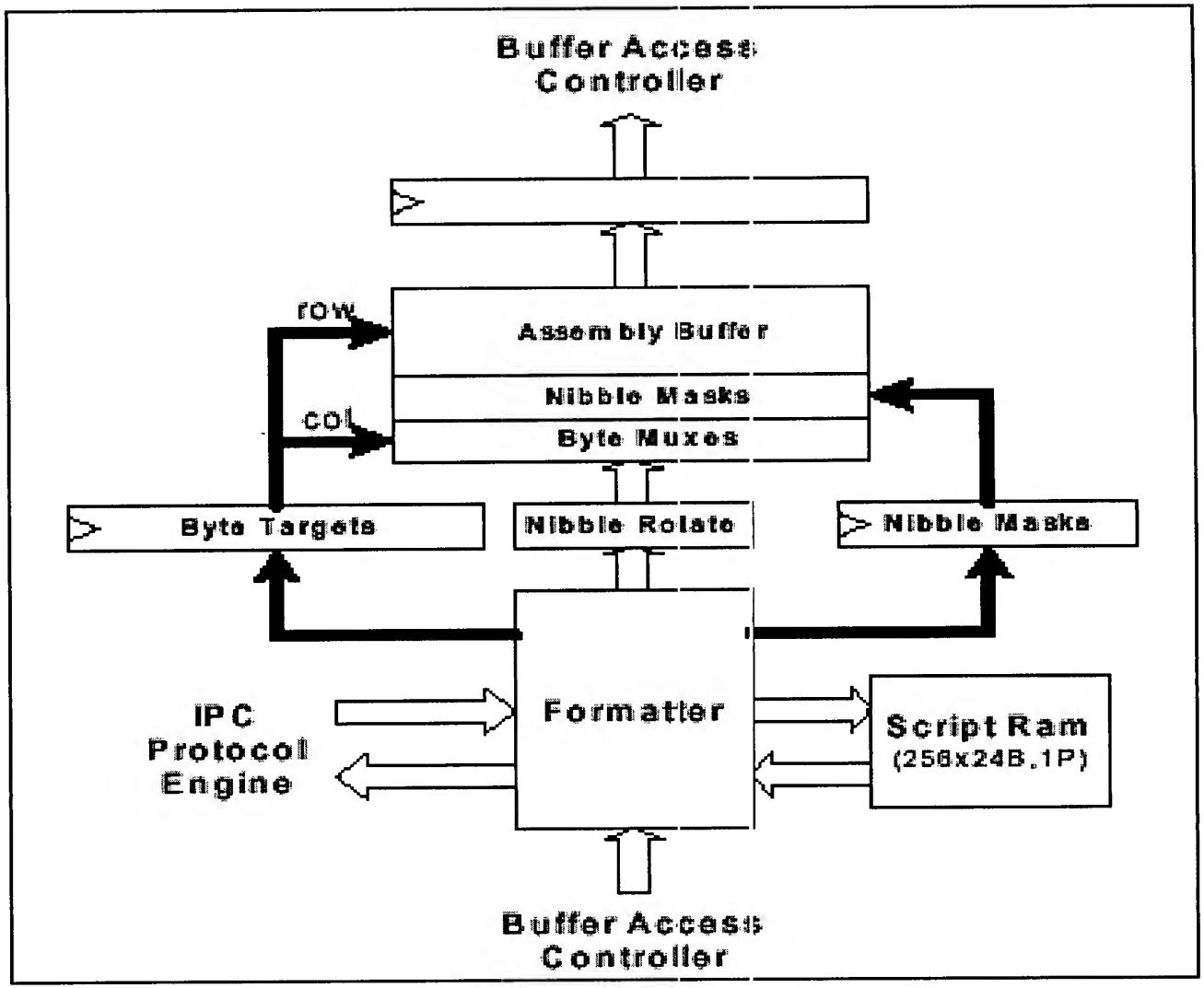


Figure 44

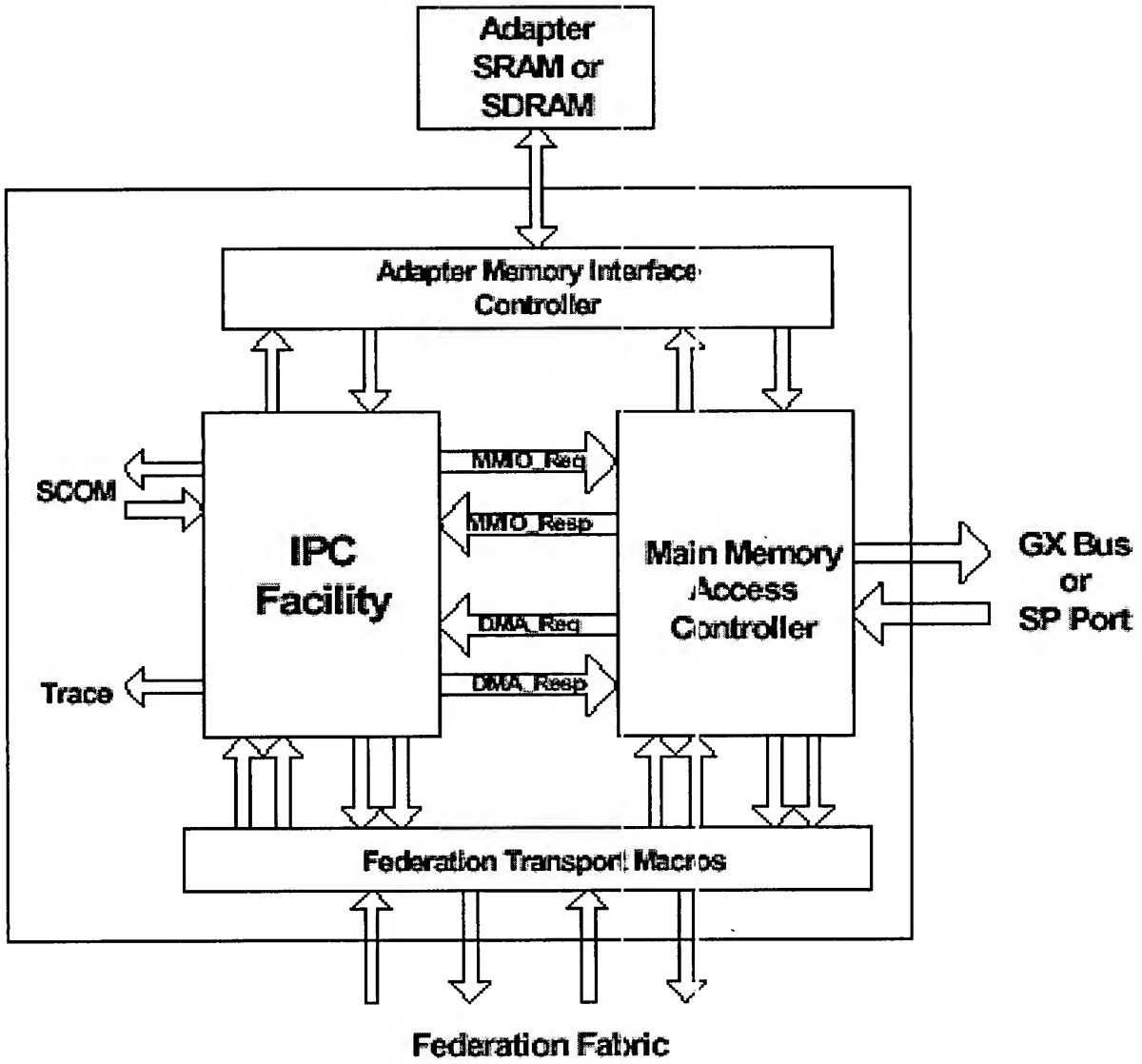

Adapter
SRAM or
SDRAM
Adapter Memory Interface
Controller
SCOM
Trace
IPC
Facility
MMIO_Req
MMIO_Resp
DMA_Req
DMA_Resp
Main Memory
Access
Controller
GX Bus
or
SP Port
Federation Transport Macros
Federation Fabric

Figure 45

Section 18

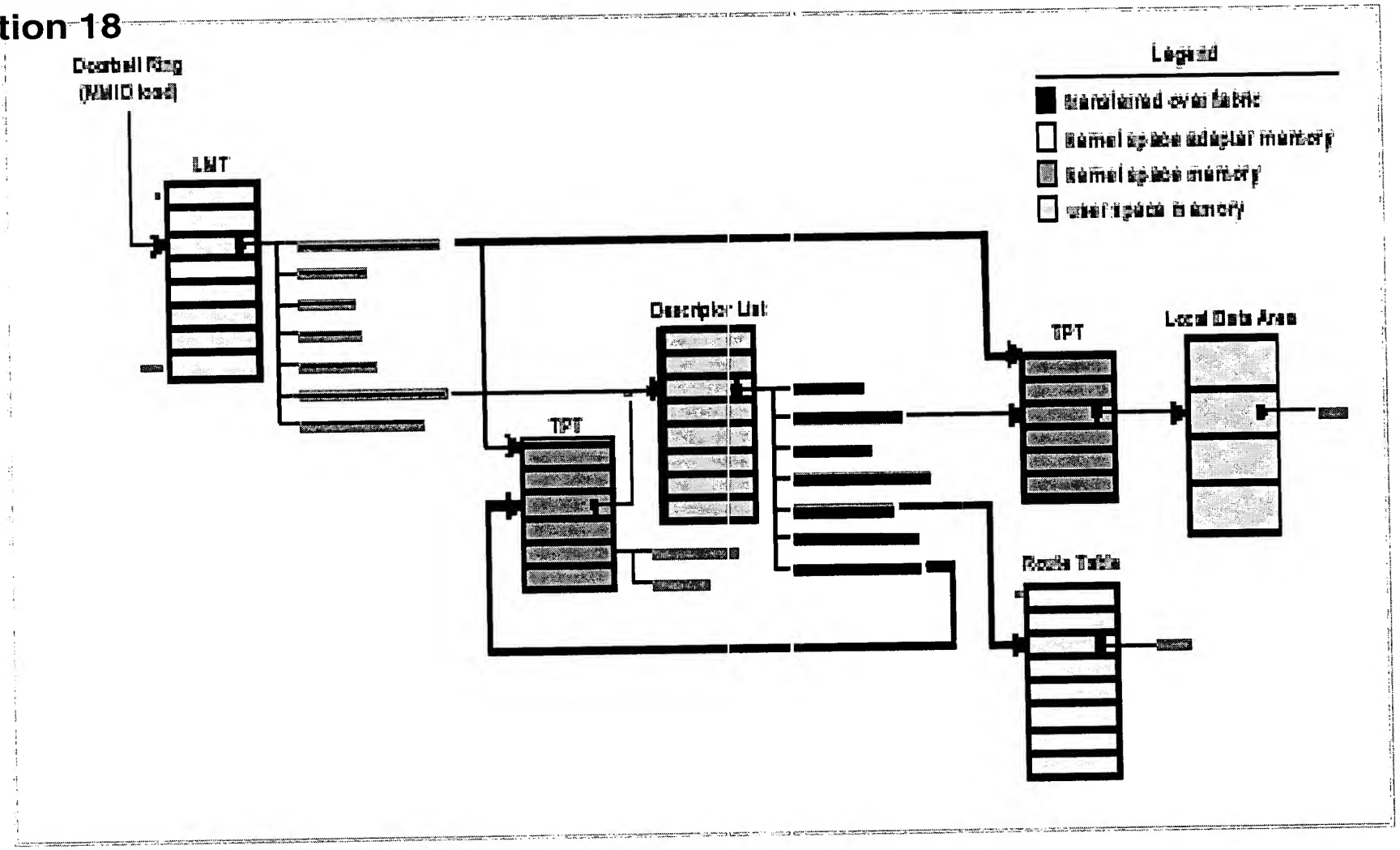


Figure 46

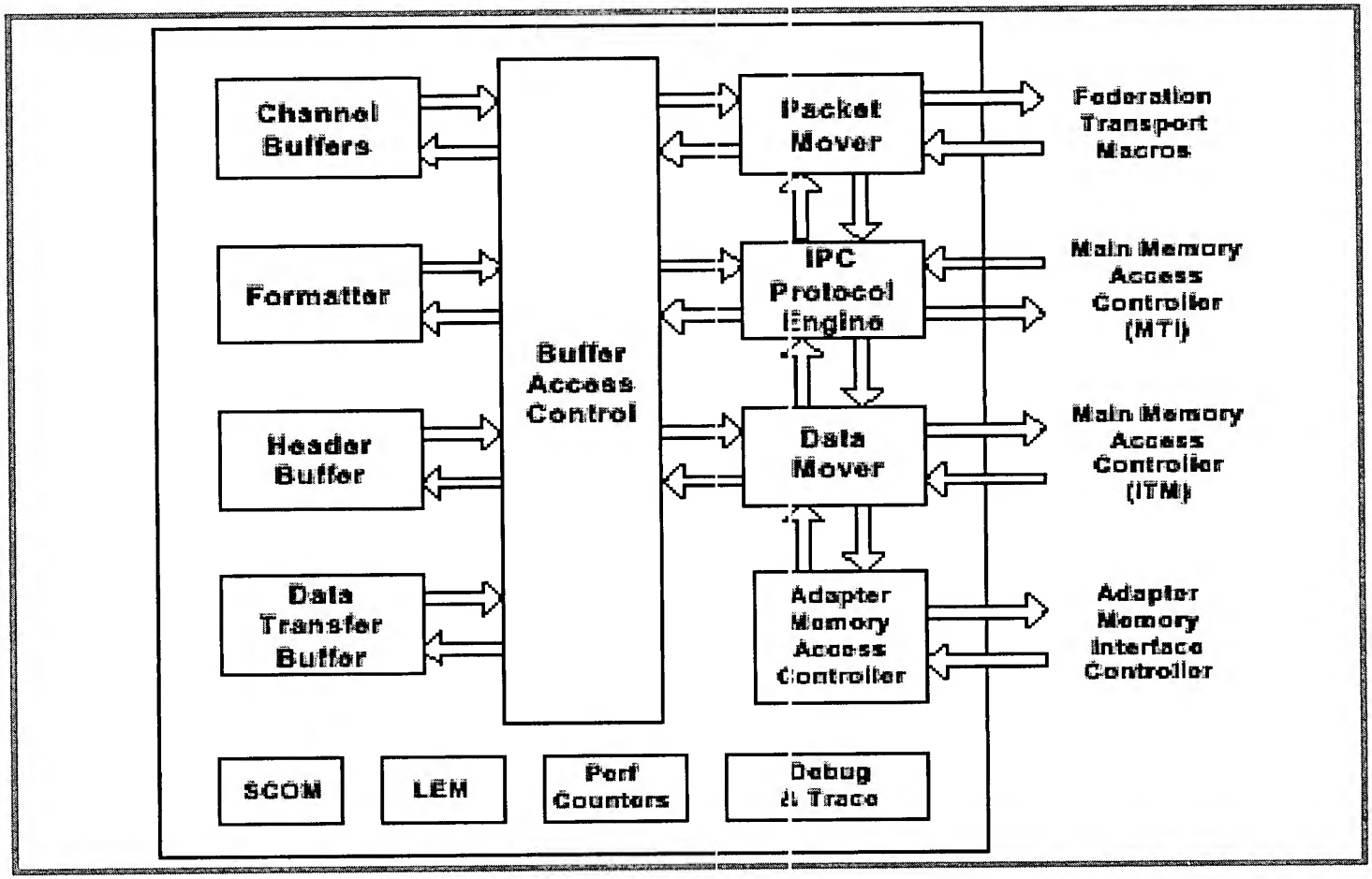

Channel Buffers
Formatter
Header Buffer
Data Transfer Buffer
Buffer Access Control
Packet Mover
IPC Protocol Engine
Data Mover
Adapter Memory Access Controller
Federation Transport Macros
Main Memory Access Controller (MTI)
Main Memory Access Controller (ITM)
Adapter Memory Interface Controller
SCOM
LEM
Perf Counters
Debug & Trace

Figure 47

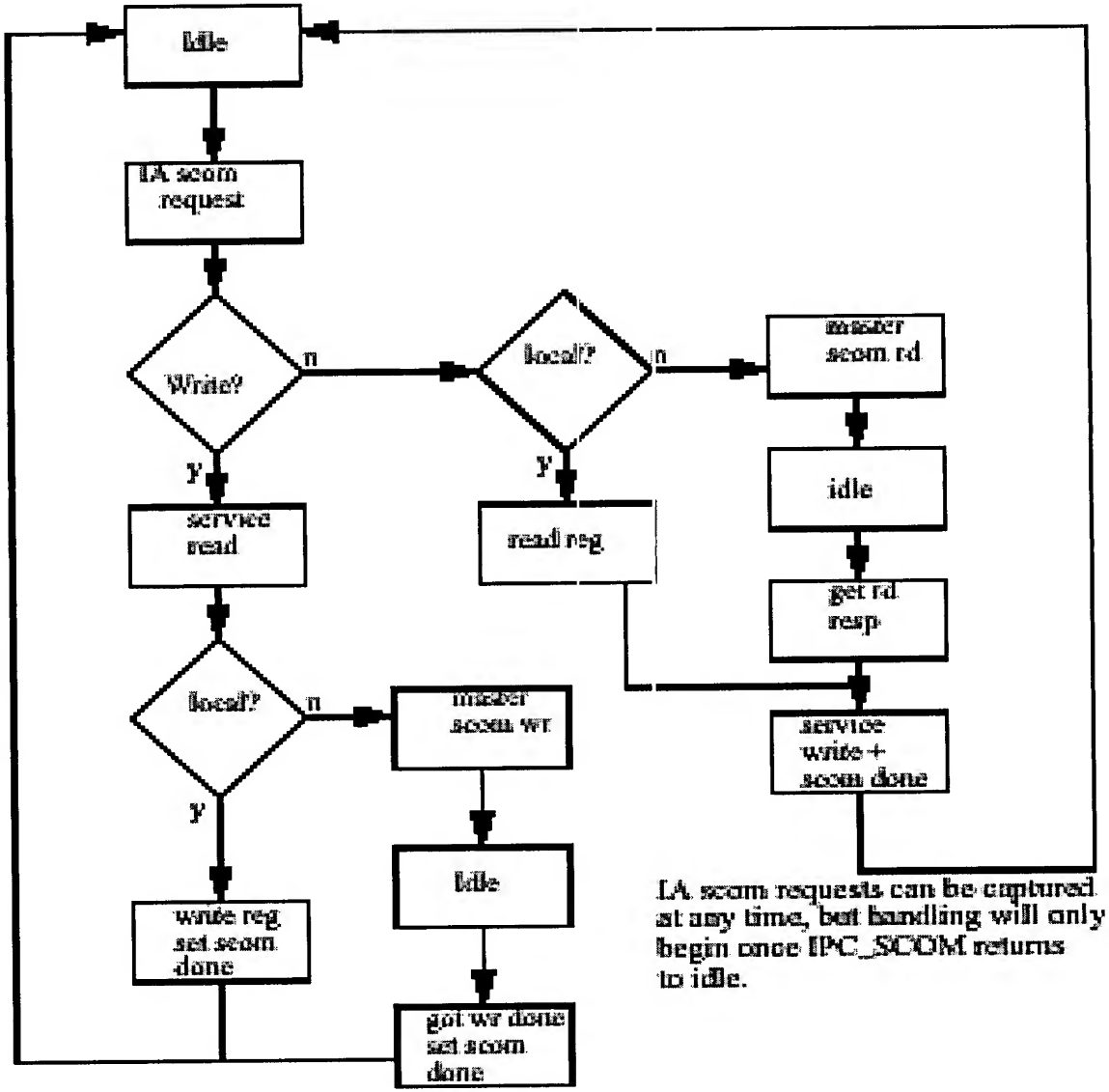

Idle
IA scom request
Write?
n
y
local?
n
y
master scom rd
idle
get rd resp
service write + scom done
service read
read reg
local?
n
y
master scom wr
idle
write reg set scom done
got wr done set scom done
IA scom requests can be captured at any time, but handling will only begin once IPC_SCOM returns to idle.

Figure 4.8

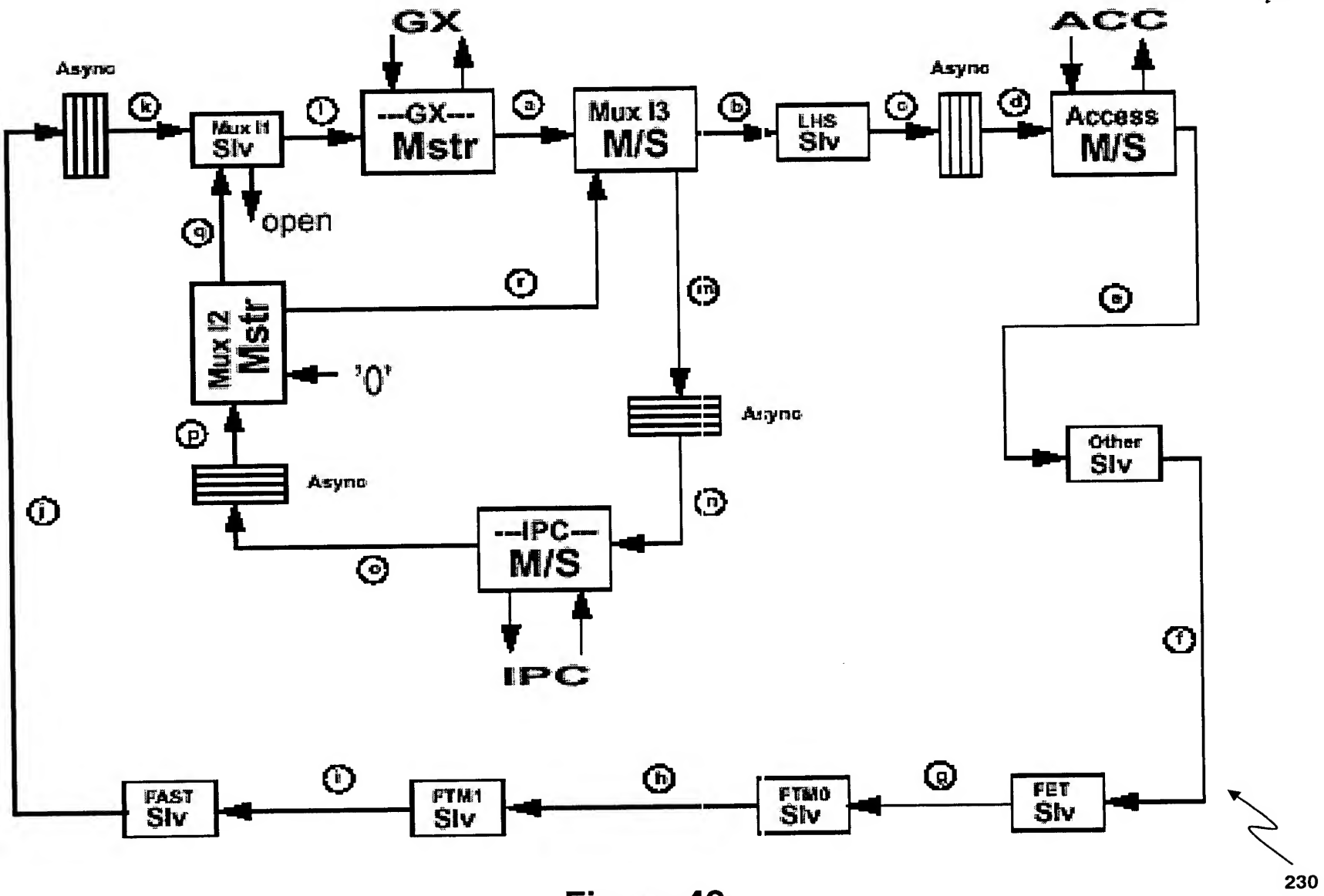

GX
ACC
Async
Async
Mux I1
Slv
---GX---
Mstr
Mux I3
M/S
LHS
Slv
Access
M/S
open
Mux I2
Mstr
'0'
Async
Async
Other
Slv
---IPC---
M/S
IPC
FAST
Slv
FTM1
Slv
FTM0
Slv
FET
Slv
230

Figure 49

IPC Protocol Engine

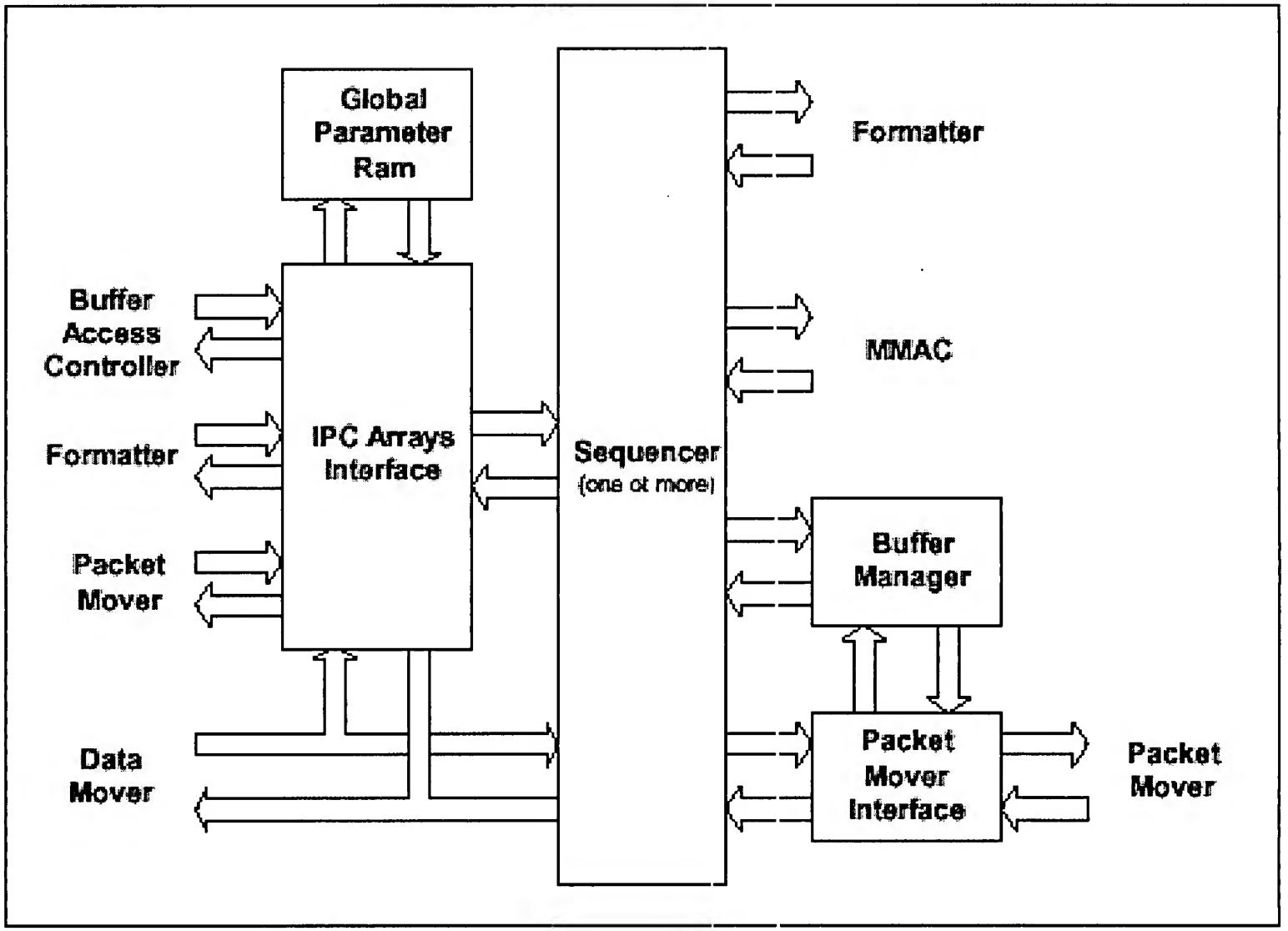


Figure 50